

#4

FIG. 1

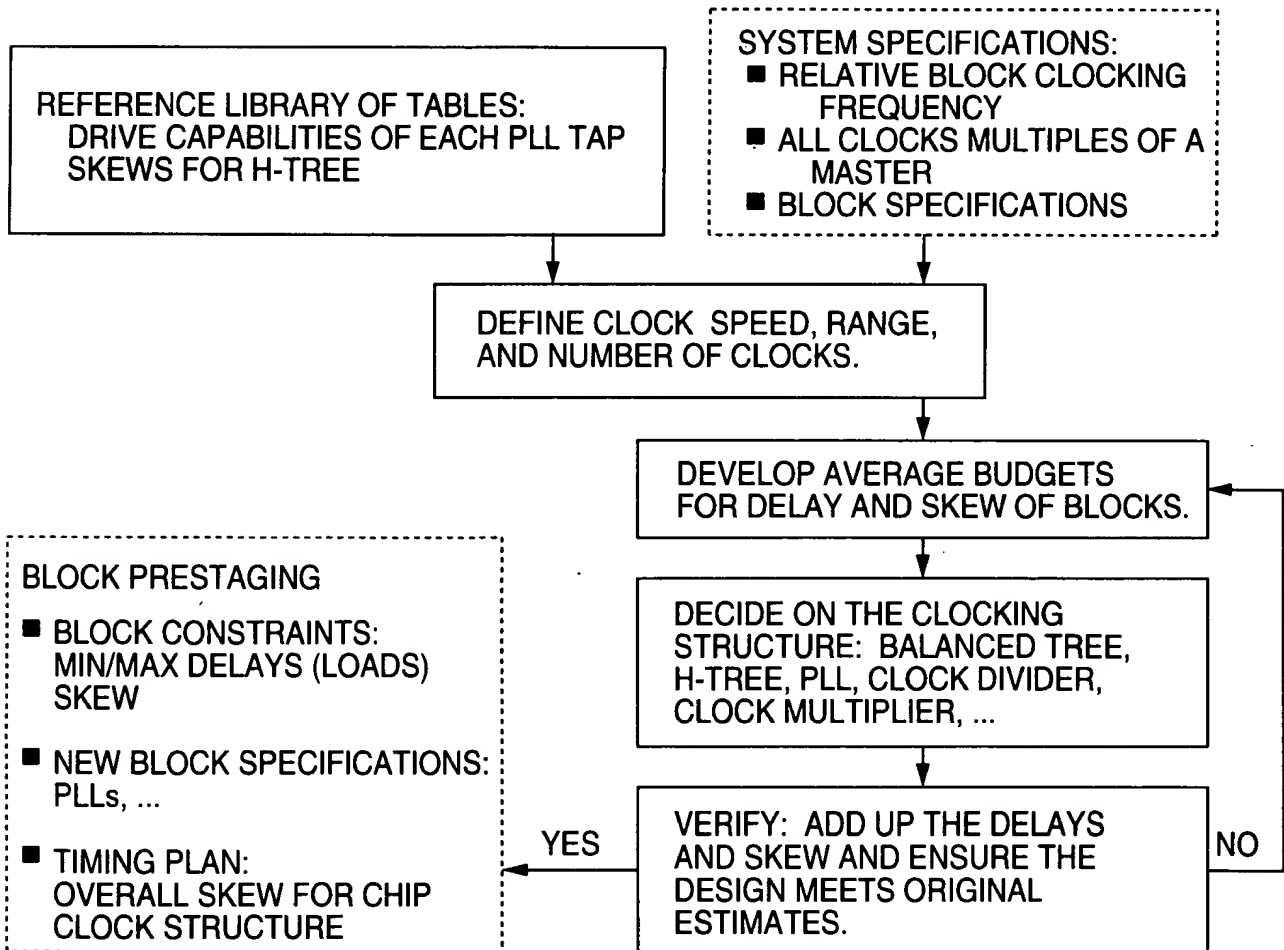
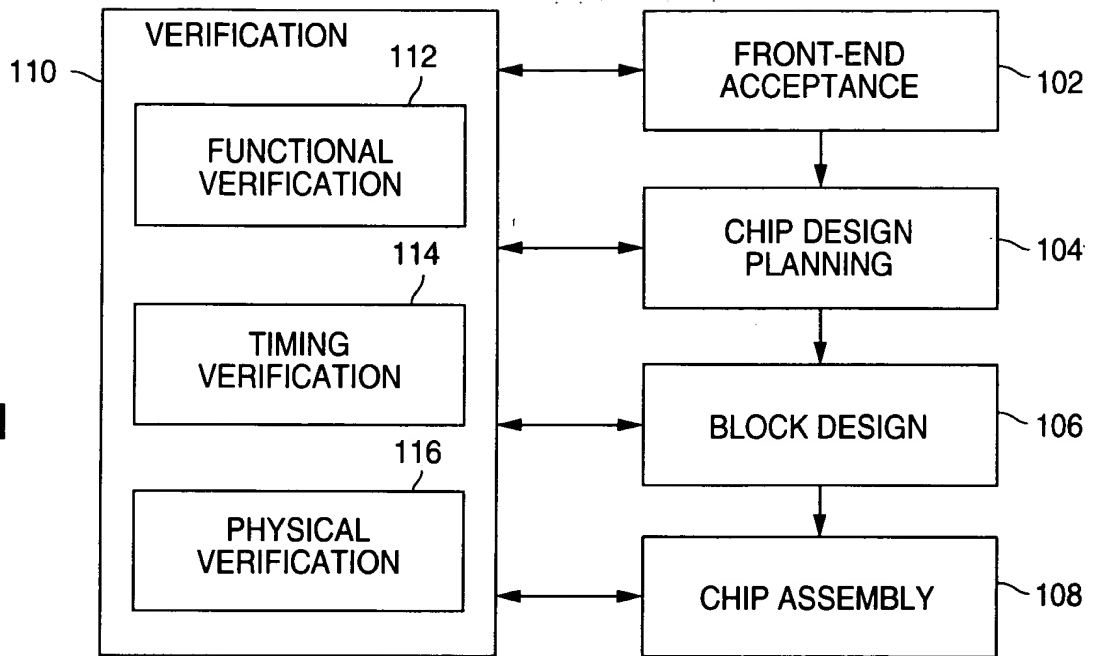
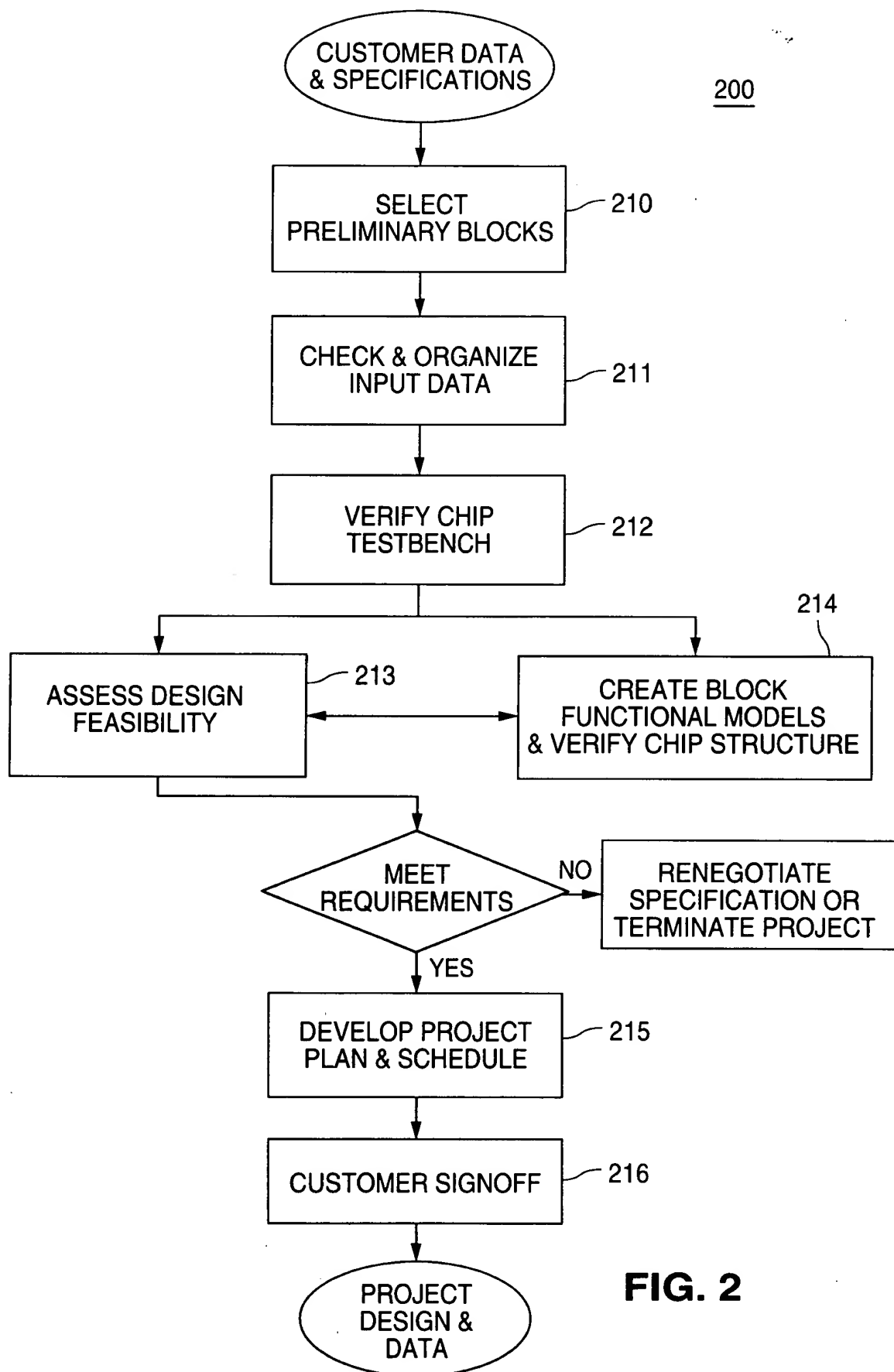
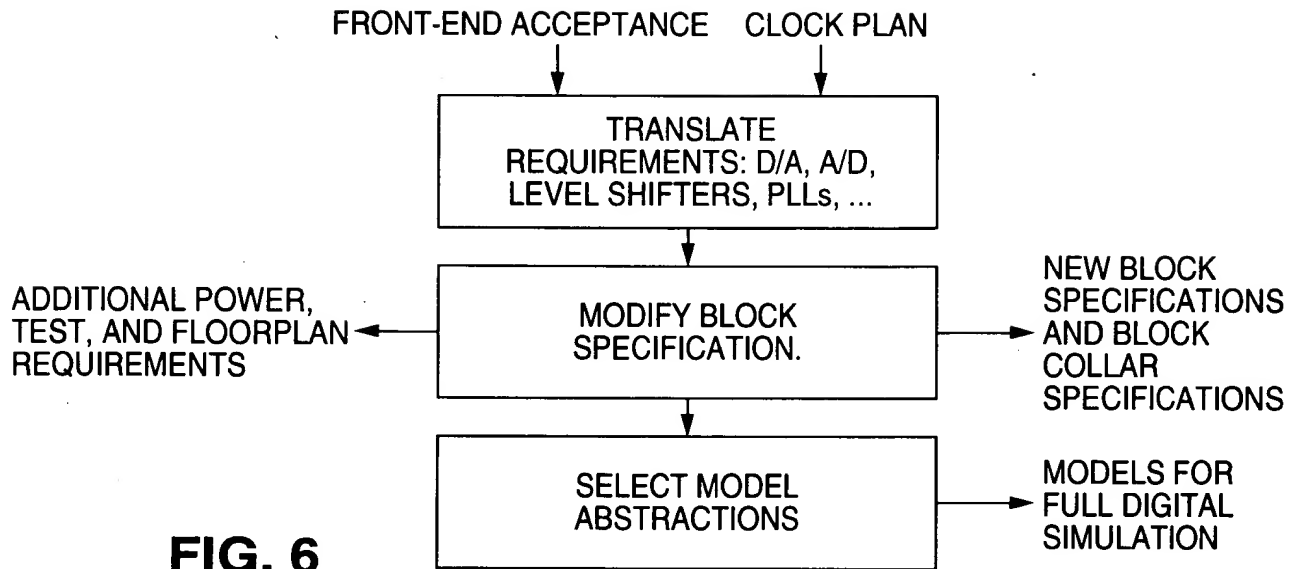


FIG. 3

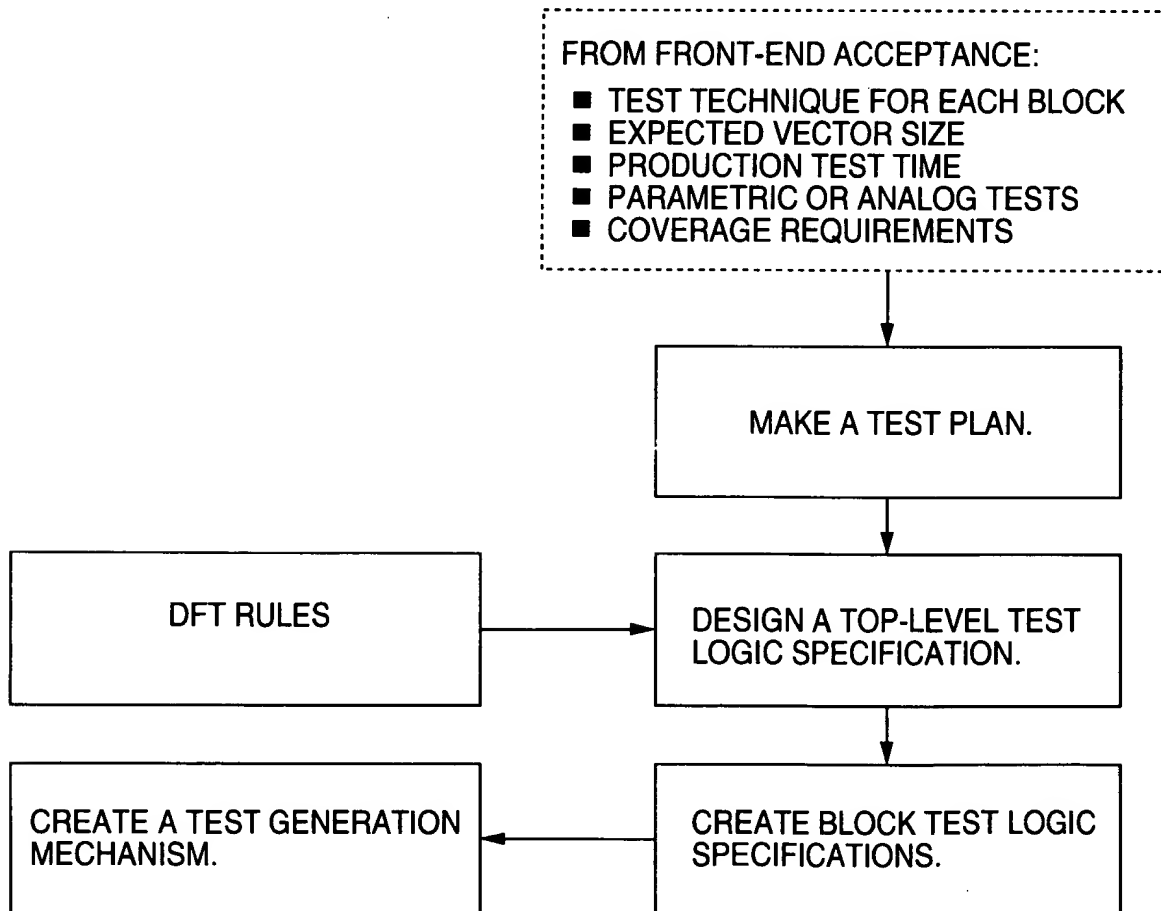


**FIG. 2**

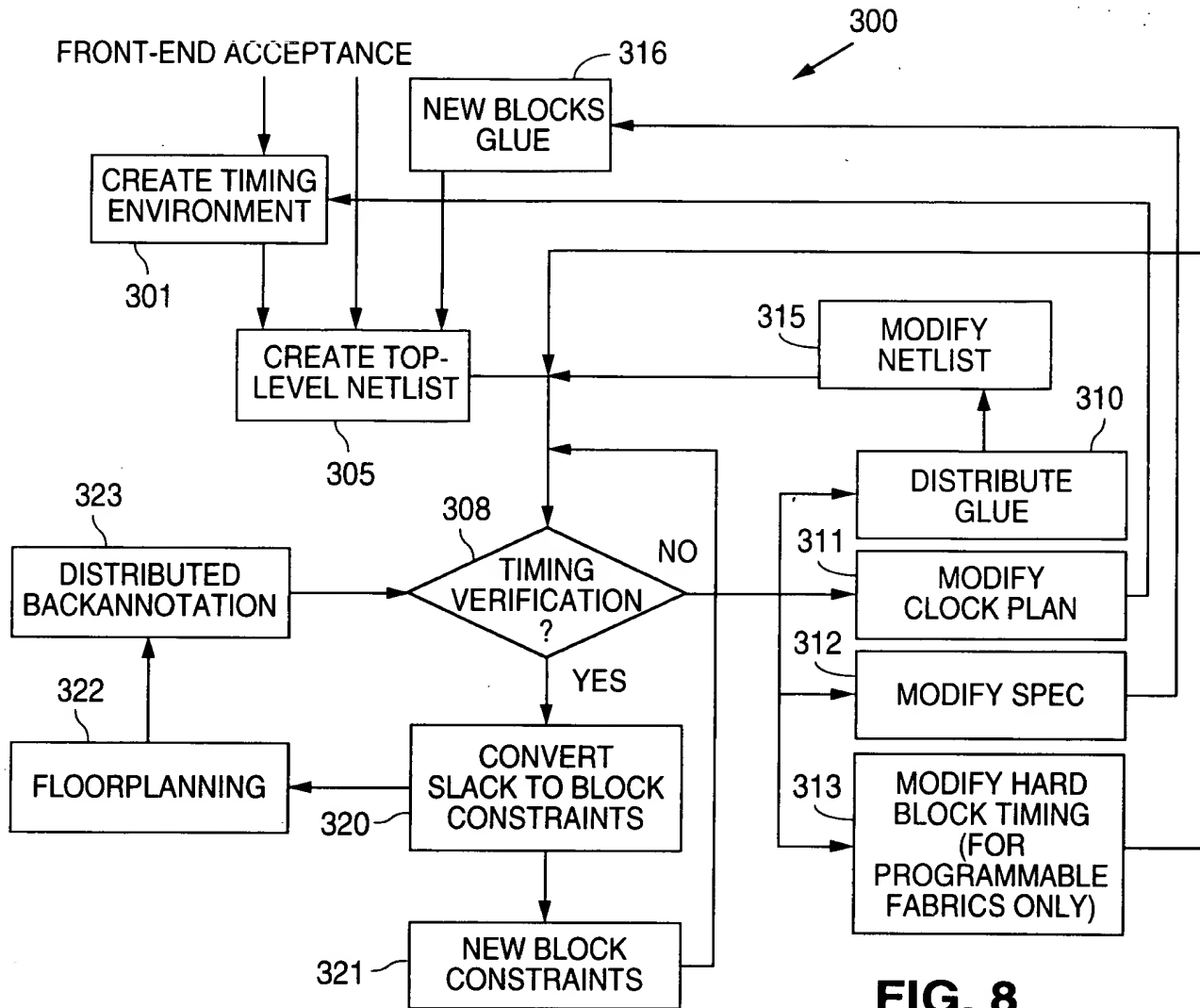




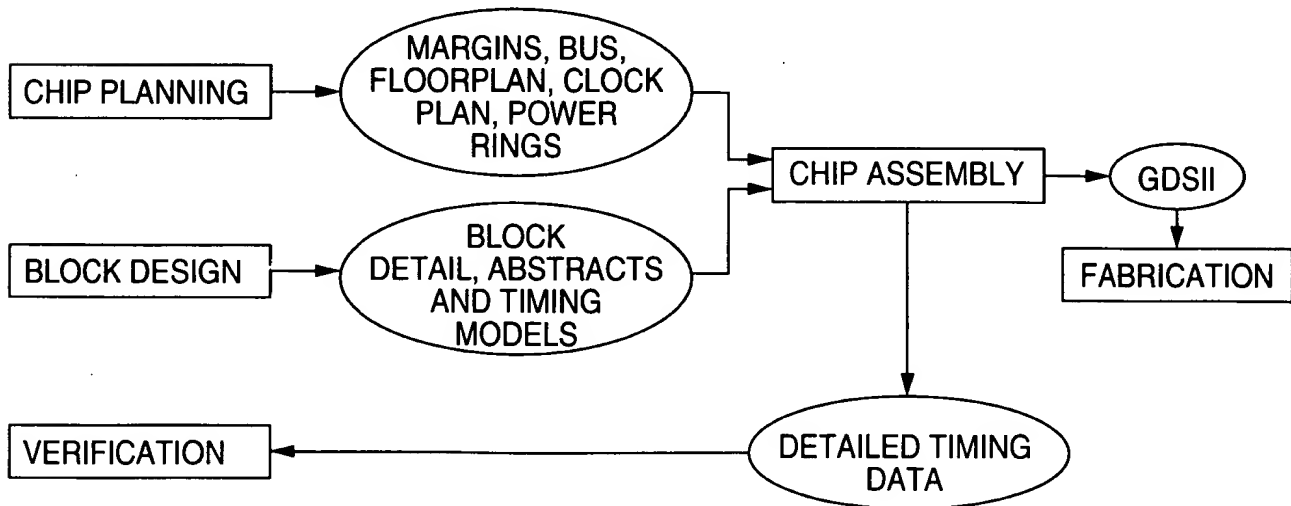
**FIG. 6**



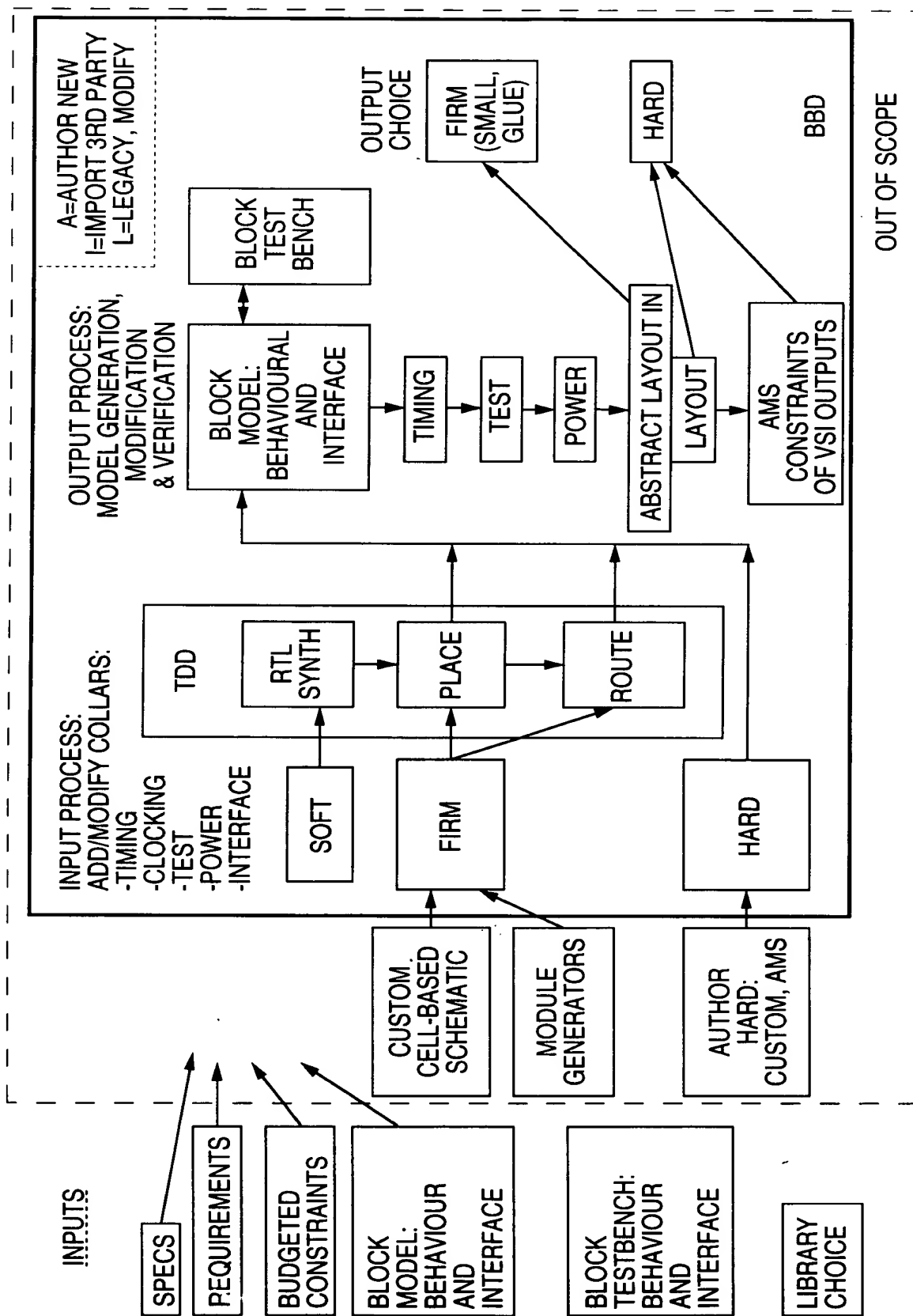
**FIG. 7**



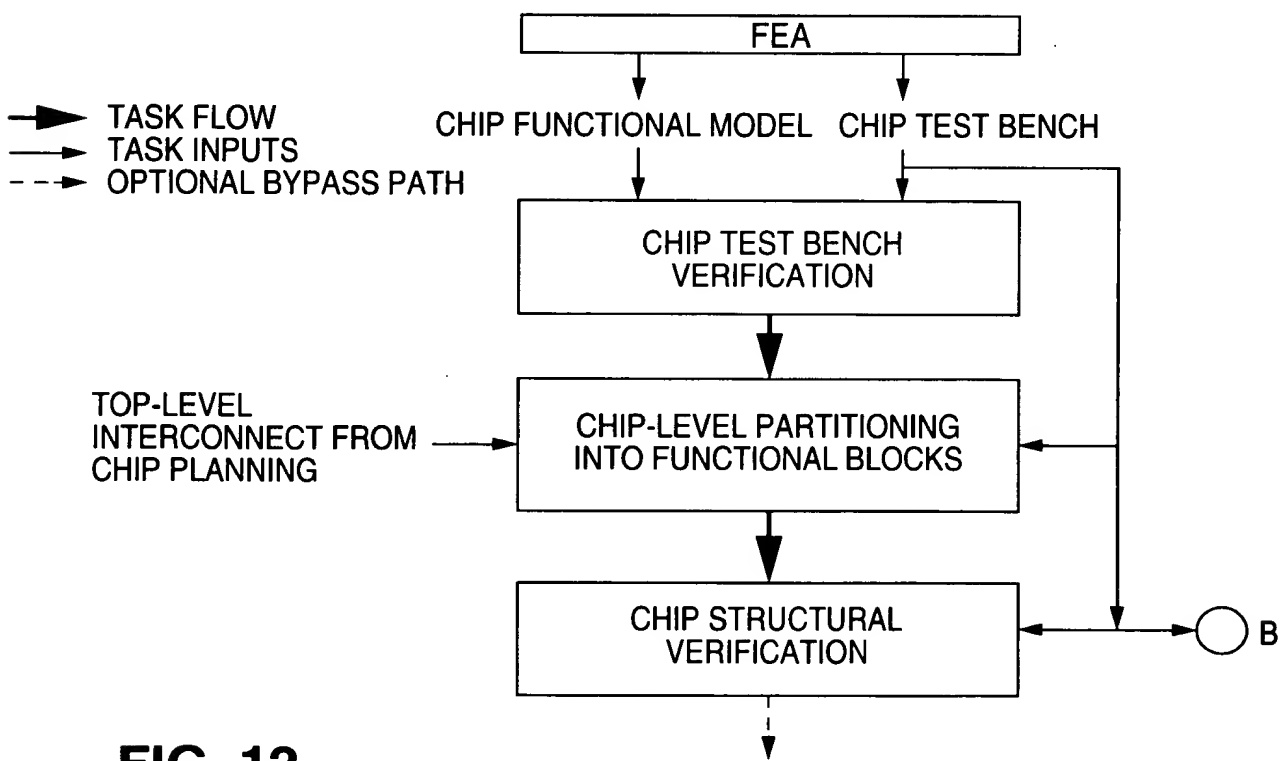
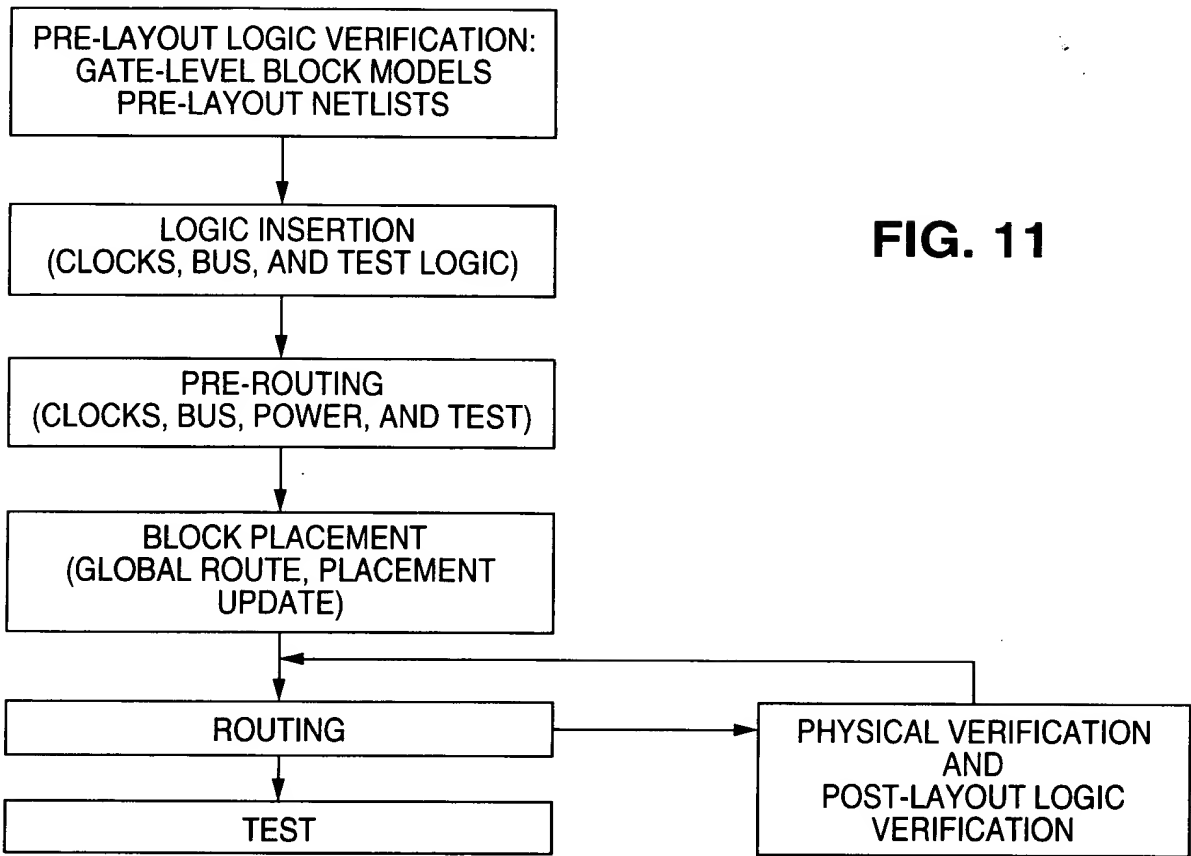
**FIG. 8**



**FIG. 10**



**FIG. 9**



AFTER FRONT-END ACCEPTANCE, BUS VERIFICATION MAY OPTIONALLY BE BYPASSED

→ TASK FLOW  
 → TASK INPUTS  
 - - - OPTIONAL BYPASS PATH

AFTER FRONT-END ACCEPTANCE BUS VERIFICATION MAY OPTIONALLY BE BYPASSED

CUSTOMER/VENDOR-SUPPLIED BUS COMPLIANCE TEST BENCHES

CREATE BUS COMPLIANCE TEST BENCH

BUS INTERCONNECT MODEL FROM CHIP PLANNING TASK

8218

VERIFY BUS FUNCTIONALITY

FIG. 13

A

→ TASK FLOW  
 → TASK INPUTS  
 - - - OPTIONAL BYPASS PATH

8610

CREATE BUS BLOCK MODELS

8614

BUS BLOCK MODELS TO BLOCK DESIGN

VERIFY BUS BLOCK MODELS

8612

BLOCK TEST BENCHES TO BLOCK DESIGN

EXTRACT BLOCK TEST BENCHES

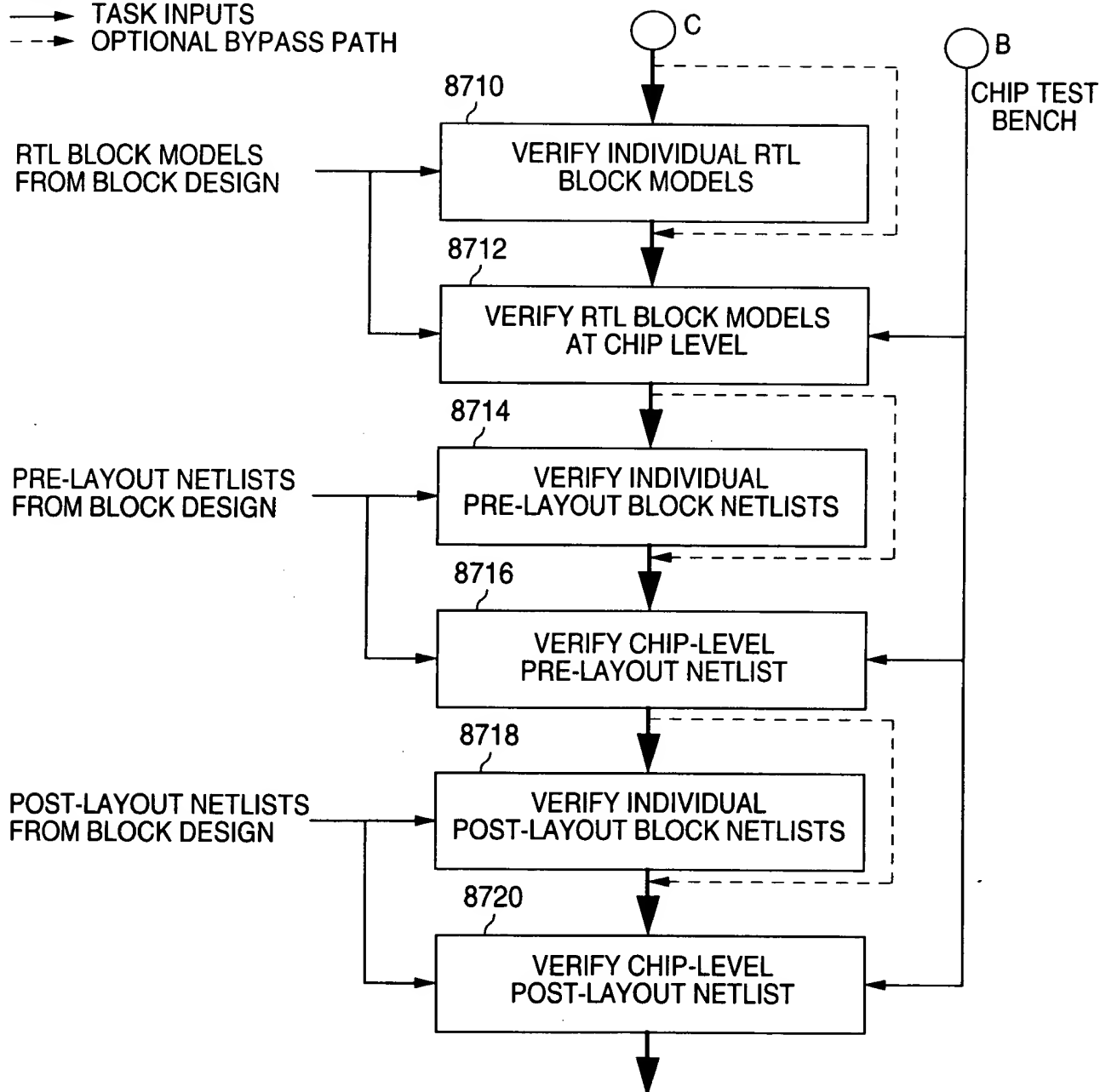
FIG. 14

C

B



→ TASK FLOW  
 → TASK INPUTS  
 --- OPTIONAL BYPASS PATH



**FIG. 15**

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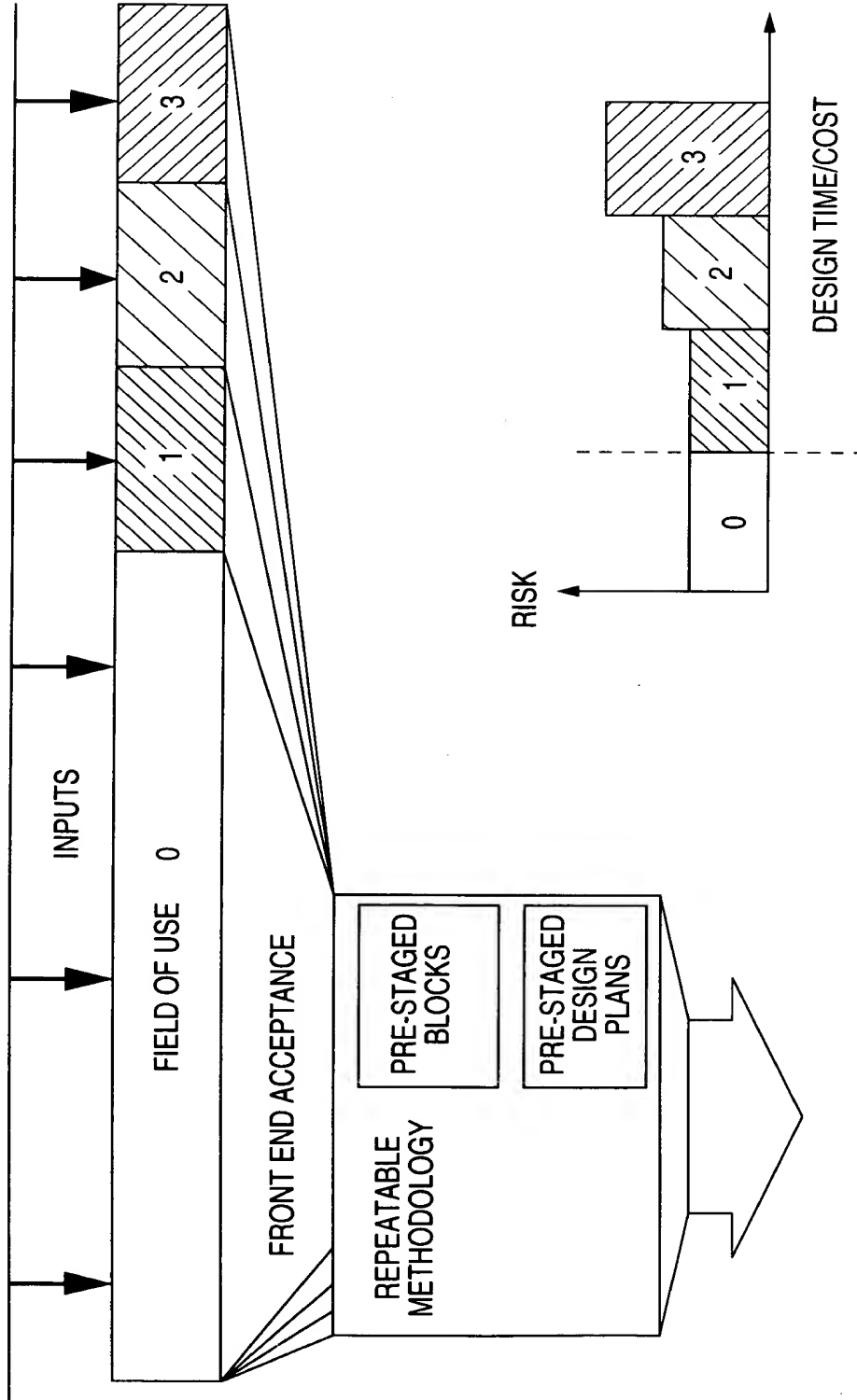
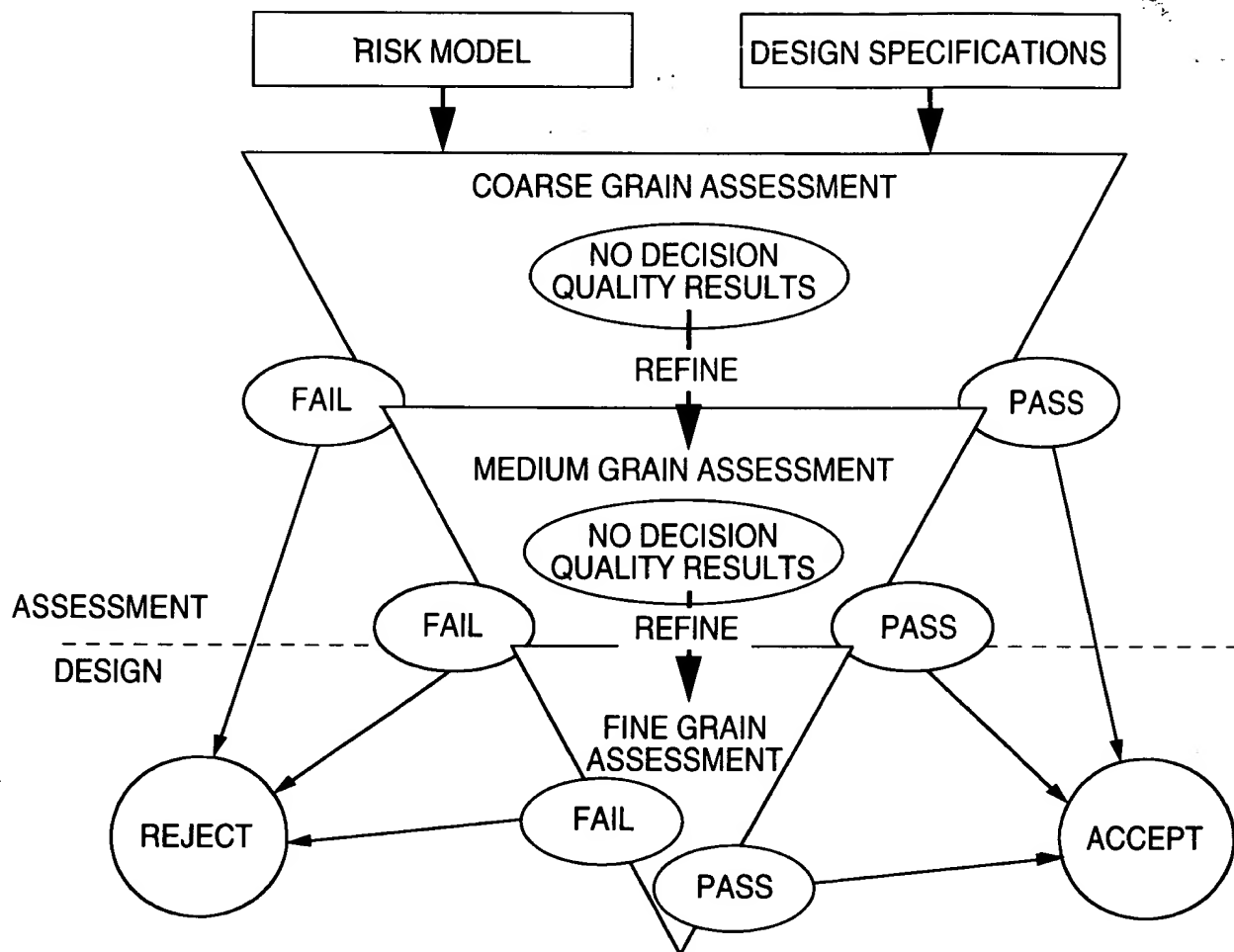


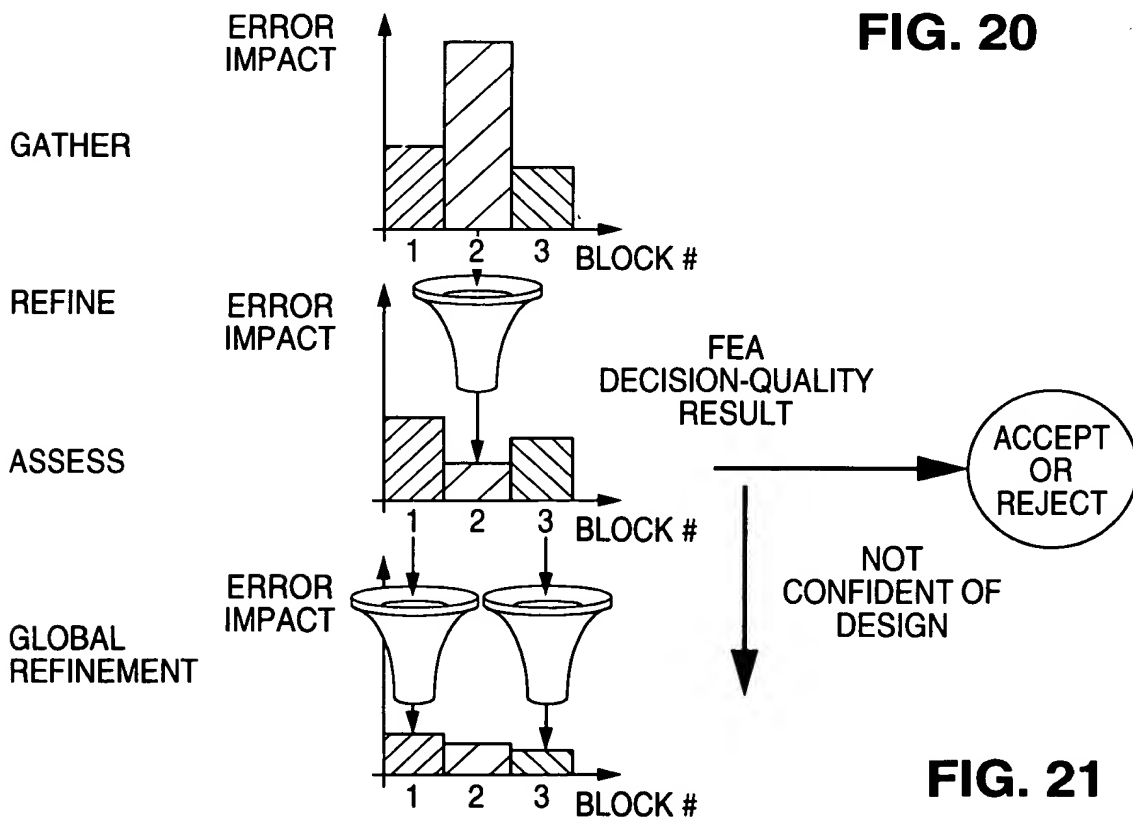
FIG. 16

FIG. 17





**FIG. 20**



**FIG. 21**

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

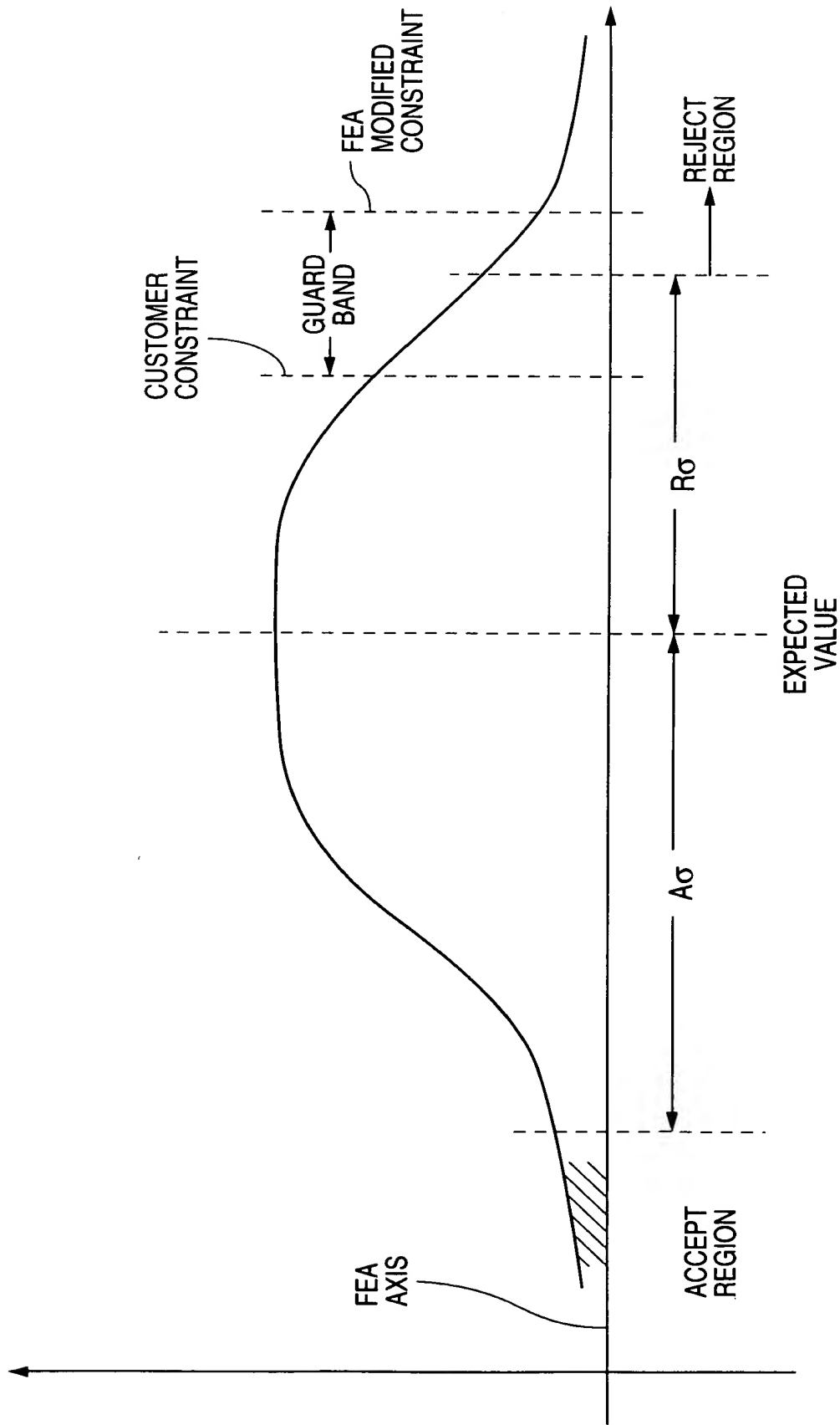


FIG. 22

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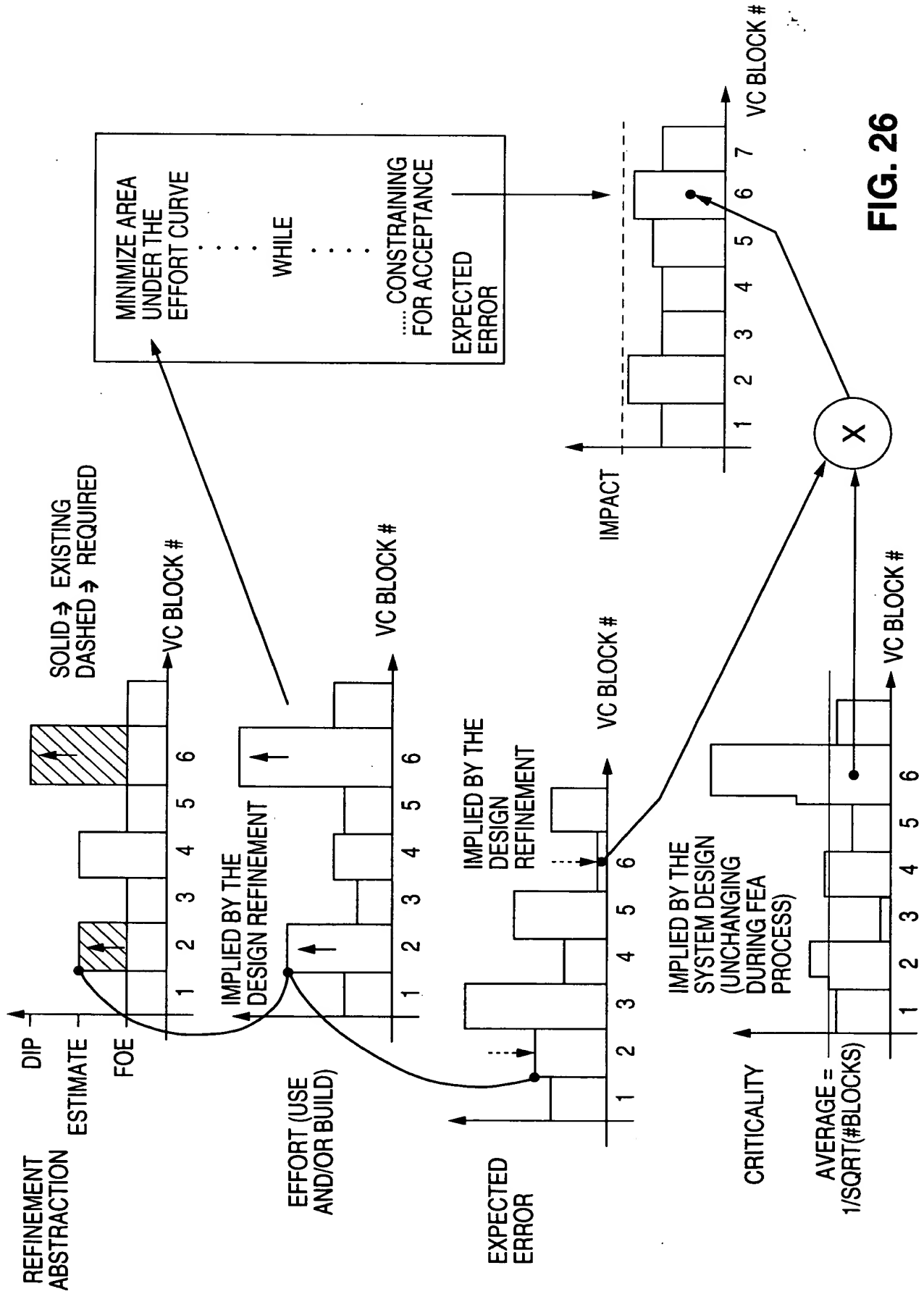


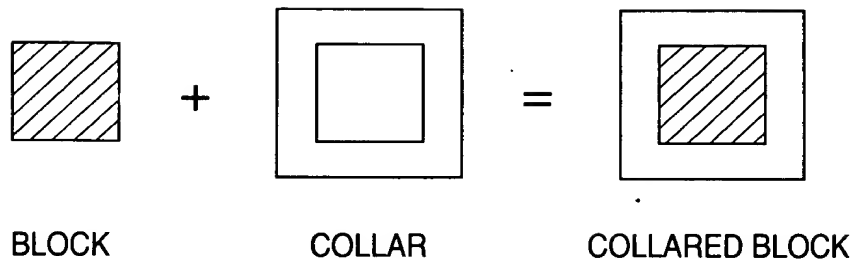


FIG. 27

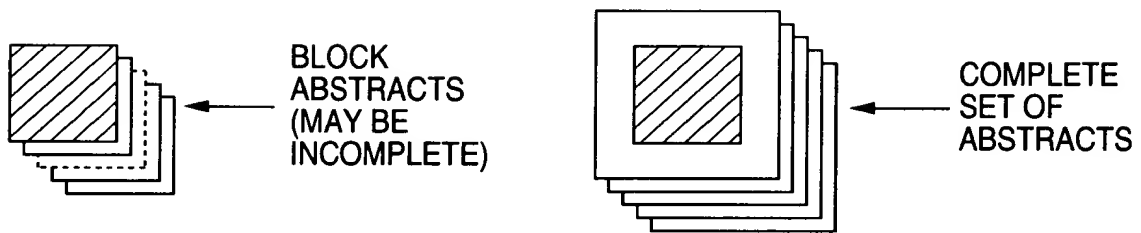
ASSESSMENT AXIS	CONSTRAINT TYPE	CONSTRAINT CLASS	ROUTING REFINEMENT	EXAMPLE CRITICALITY MEASURES
POWER	PER MODE OF OPERATION	RELATIVE	MEDIUM	(EXPECTED-BLOCK-POWER ERROR)+ (BLOCK-ROUTING CRITICALITY) * 0.5 * V <sup>2</sup> * E <sub>BLOCK</sub>
PERFORMANCE	TRANSPORT DELAY	ABSOLUTE	FINE	N/A (I.E., LOCAL-CONNECTION NOT A SYSTEM-SUMMED CRITERIA)
	LATENCY	RELATIVE	MEDIUM	CRITICALITY OF LATENCY-PATH TO SYSTEM: 1/(((1-Pr(STARVATION))* ((REQUIRED PATH-LATENCY- (Σ (BLOCK LATENCY) + Σ (BUS LATENCY)))) CRITICALITY OF BLOCK TO LATENCY PATH: (LATENCY ERROR) / (1-Pr(STARVATION)))
	THROUGHPUT	ABSOLUTE	COARSE	N/A (I.E., DOMINATED BY SINGLE BOTTLE-NECK BLOCKS)
AREA	AREA	RELATIVE	MEDIUM	(AREA ERROR) + (BLOCK-ROUTING CRITICALITY)*α
COST	NRE	RELATIVE	COARSE	
	COST PER UNIT	RELATIVE	COARSE	
	RESOURCE ALLOCATION	MIXED	COARSE	
SCHEDULE	DELIVERY TIMELINES	RELATIVE	COARSE	
	POSSIBILITY OF ERROR	MIXED	COARSE	
	IMPACT OF ERROR	MIXED	COARSE	

FIG. 27

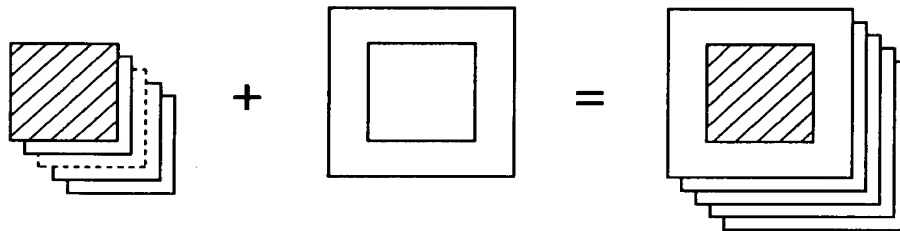




**FIG. 32**

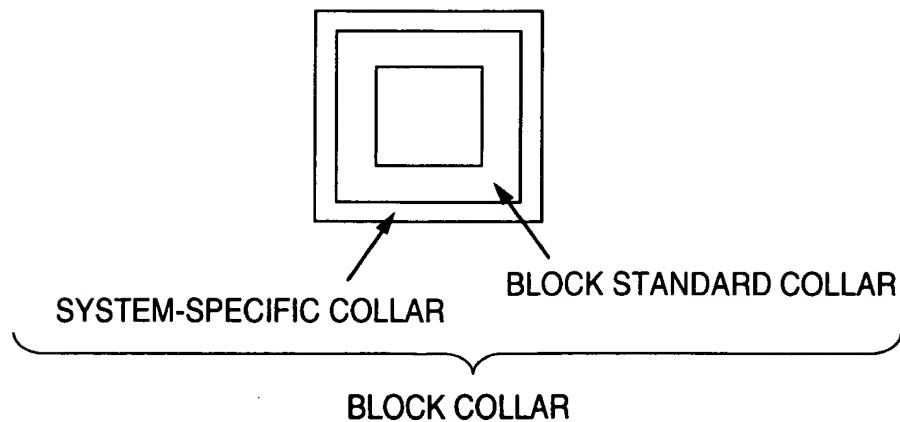


**FIG. 33**



**FIG. 34**

**FIG. 35**



00842068-012303

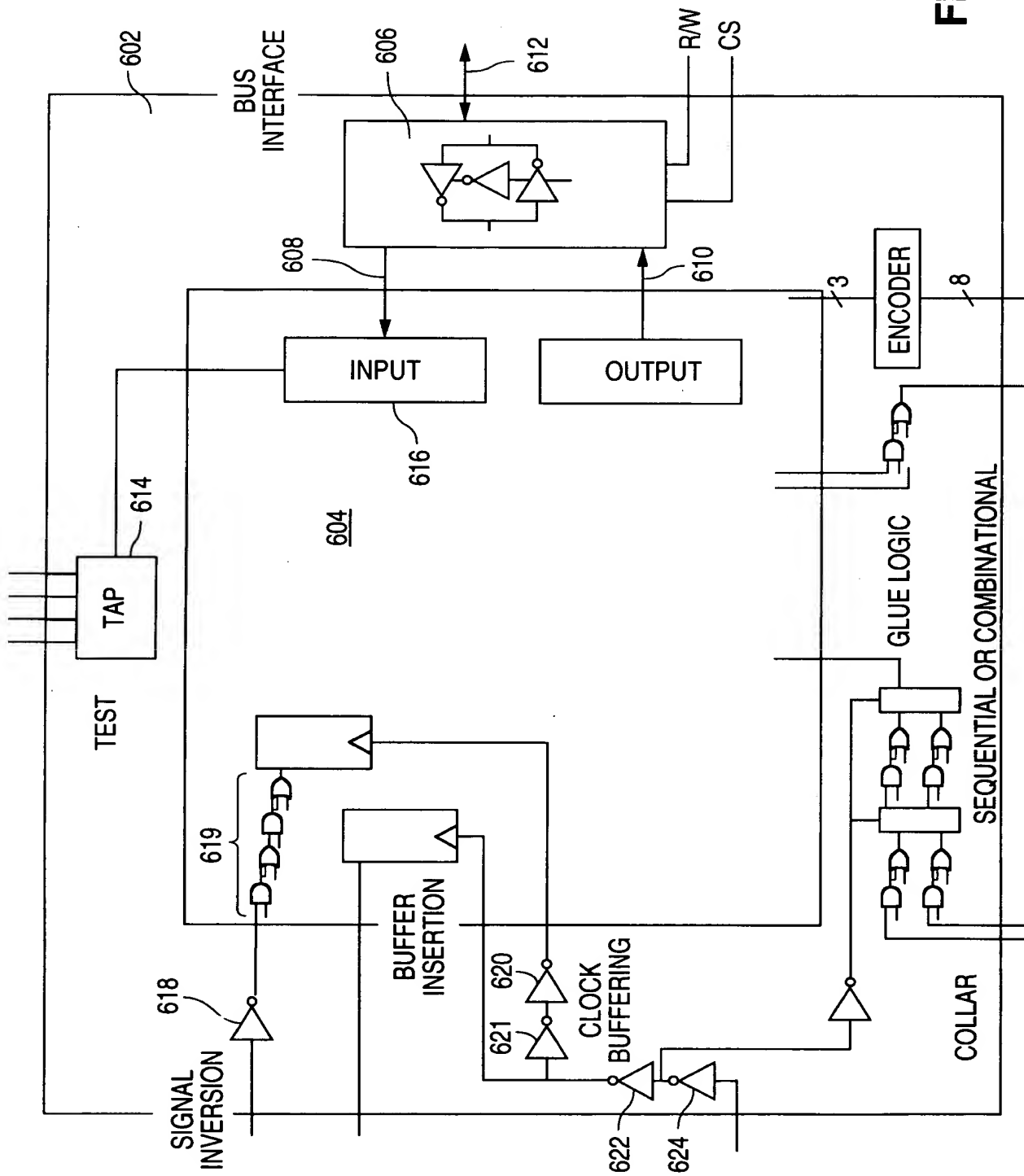
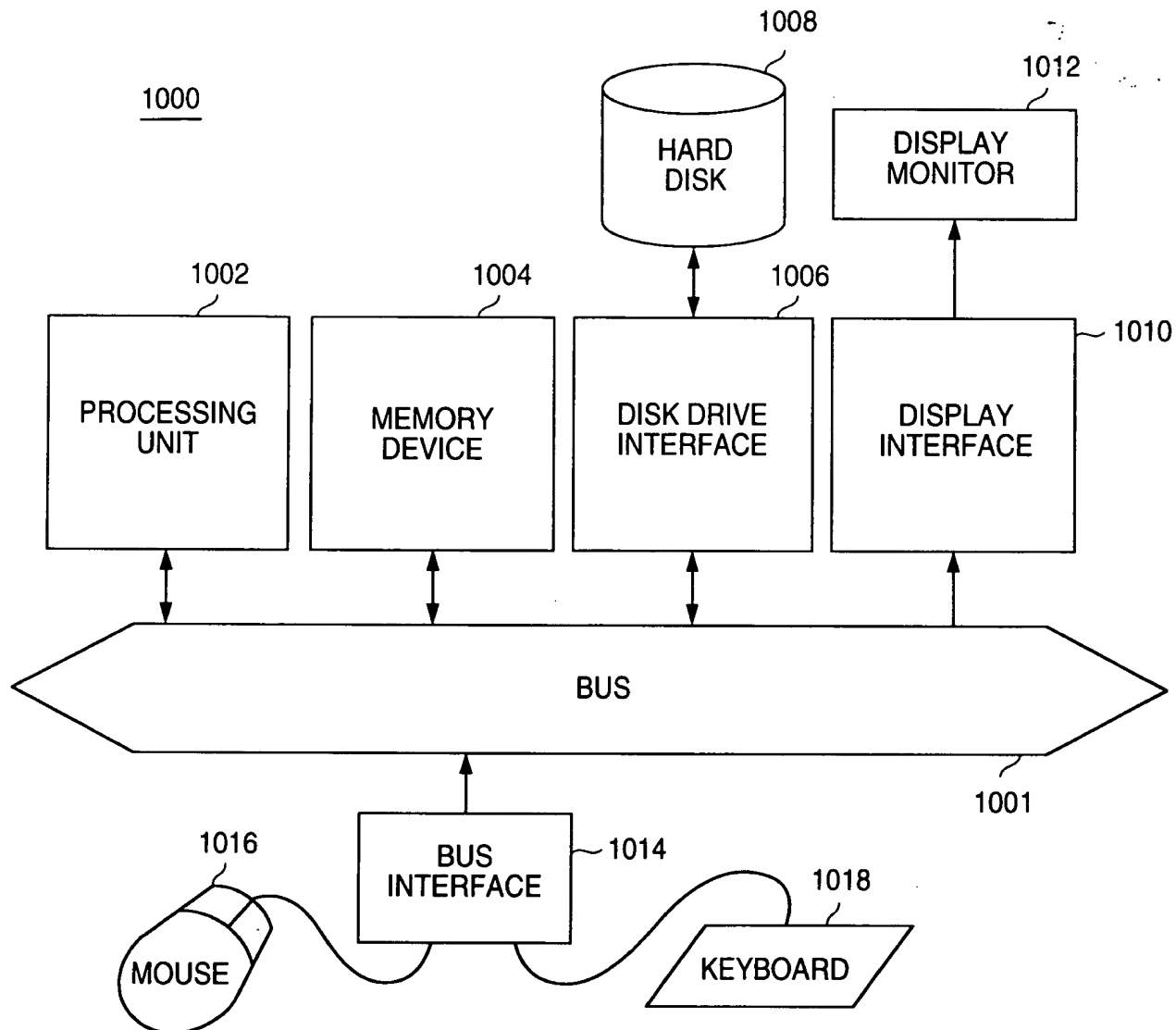


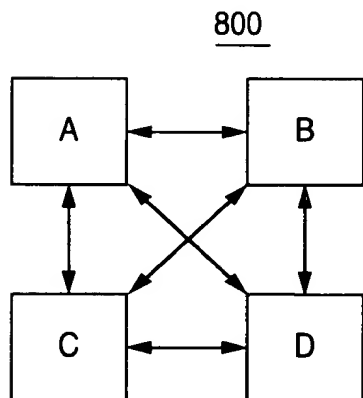
FIG. 36

2025-10-10 10:30:10

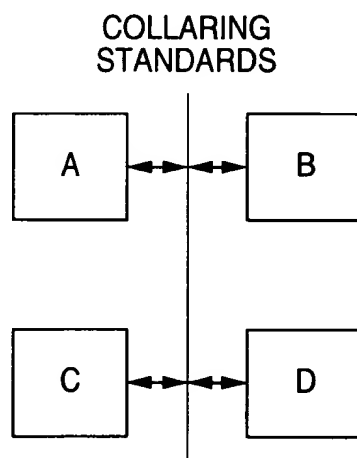




**FIG. 38**

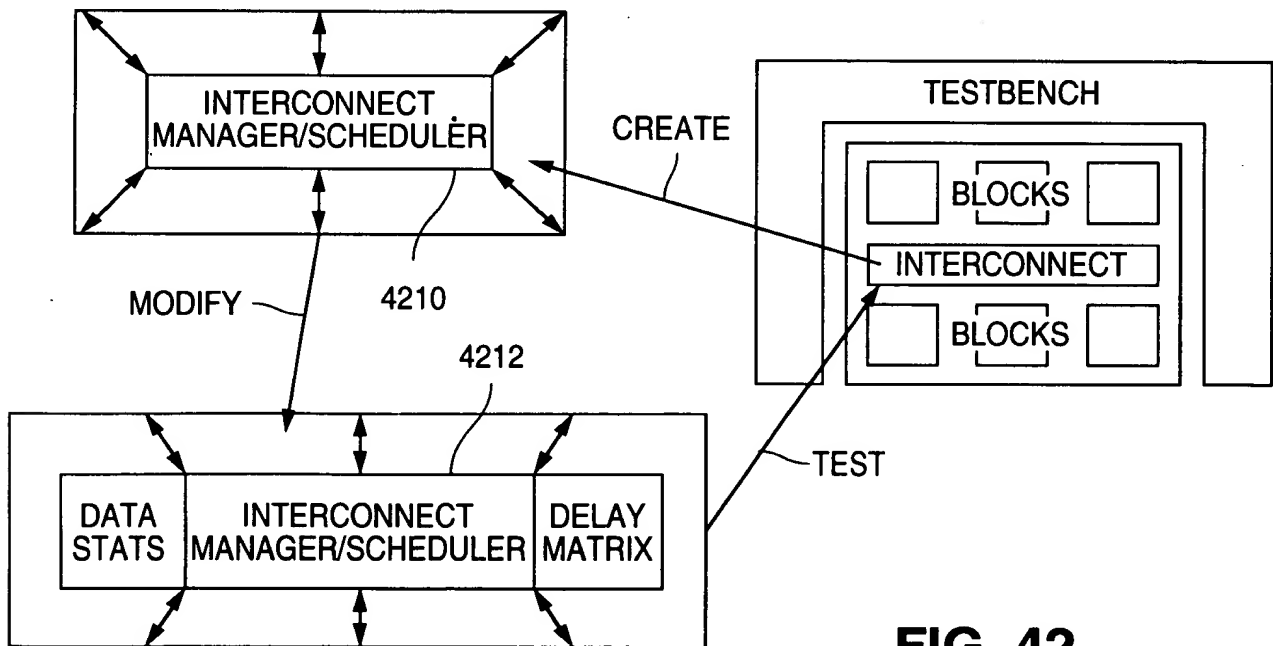
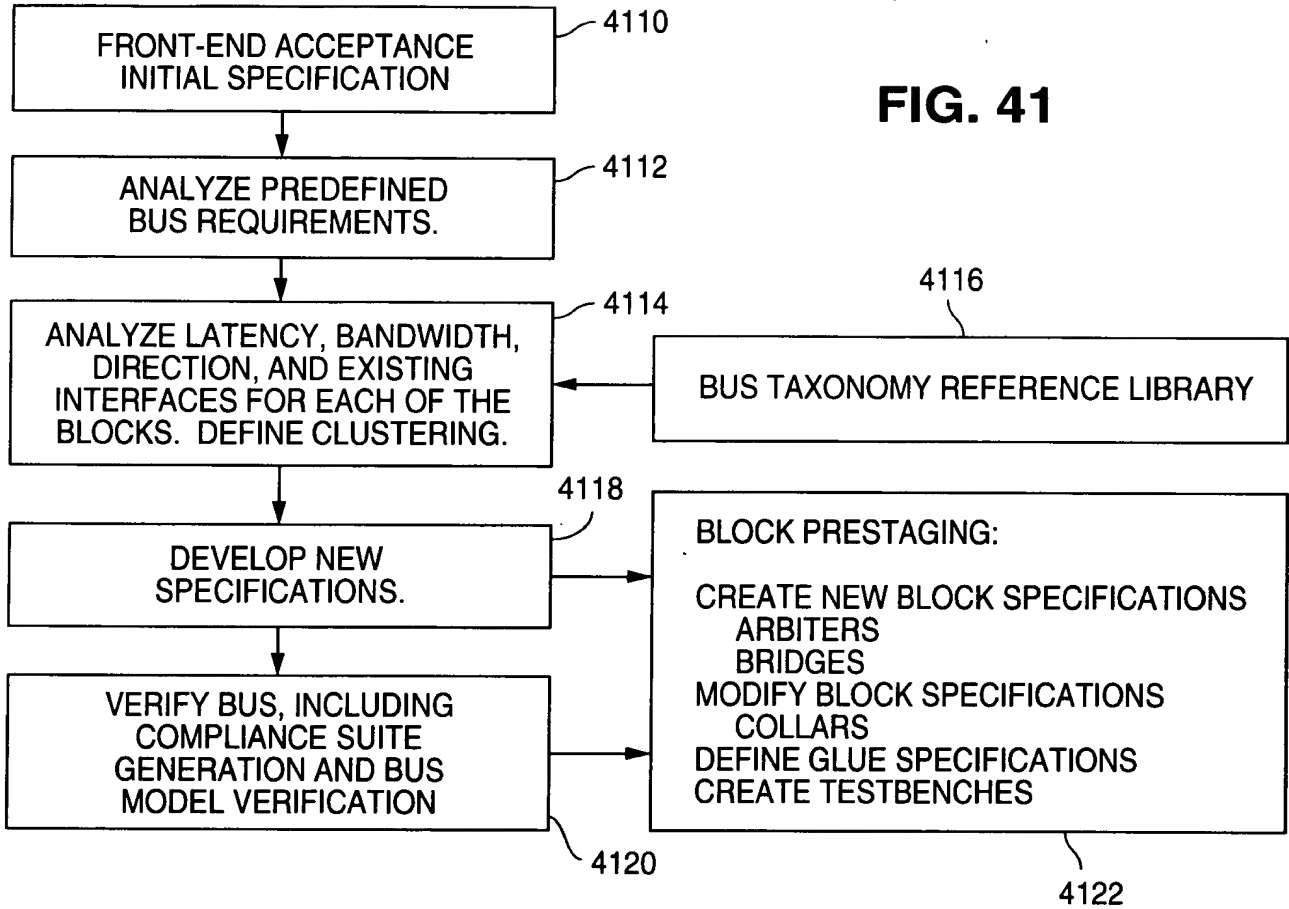


**FIG. 39**



**FIG. 40**

**FIG. 41**



**FIG. 42**

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FROM	TO					
	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	0	10,000	100	10,000	100	100
BLOCK 2	8,000	0	100	2,000	10,000	100
BLOCK 3	200	100	0	100	200	100
MEMORY	6,000	6,000	100	0	100	100
PCI	6,100	4,100	0	200	0	0
PIO	0	0	0	0	0	0

**FIG. 43**

FROM	TO					
	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	0	200	25	200	4	25
BLOCK 2	160	0	100	40	200	25
BLOCK 3	25	100	0	25	25	25
MEMORY	120	180	25	0	6	25
PCI	122	82	0	50	0	0
PIO	0	0	0	0	0	0

**FIG. 44**

FROM	TO					
	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	n/a	50	1,000	50	100	1,000
BLOCK 2	50	n/a	1,000	300	100	1,000
BLOCK 3	1,000	1,000	n/a	500	500	1,000
MEMORY	50	50	500	n/a	100	1,000
PCI	100	100	n/a	50	n/a	n/a
PIO	n/a	n/a	n/a	n/a	n/a	n/a

**FIG. 45**

FROM	TO					
	SITE 1	SITE 2	SITE 3	SITE 4	SITE 5	SITE 6
SITE 1	0	1	4	9	16	25
SITE 2	1	0	1	4	9	16
SITE 3	4	1	0	1	4	9
SITE 4	9	4	1	0	1	4
SITE 5	16	9	4	1	0	1
SITE 6	25	16	9	4	1	0

**FIG. 46**

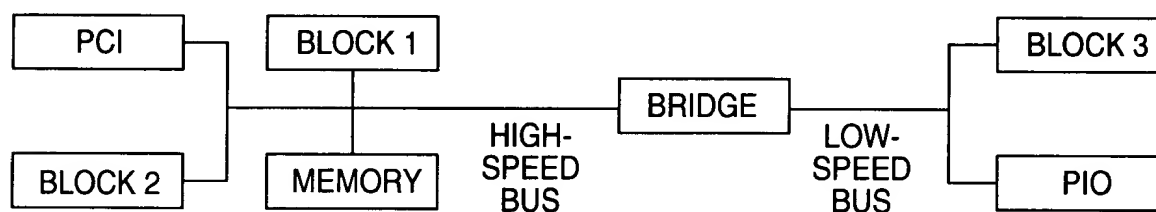
2025 RELEASE UNDER E.O. 14176



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FROM	TO	PC1	BLOCK 2	BLOCK 1	MEMORY	BLOCK 3	PIO
PCT		0	4,100	6,100	200	0	0
BLOCK 2		10,000	0	8,000	2,000	100	100
BLOCK 1		100	10,000	0	10,000	100	100
MEMORY		100	6,000	6,000	0	100	100
BLOCK 3		200	100	200	100	0	100
PIO		0	0	0	0	0	0

**FIG. 47**



**FIG. 48**

FROM	TO	A	B	C	D	E	F	G	H
A		0	##	##					
B		##	0	##					
C		##	##	0					
D					0	##			
E					##	0	##		
F						##	0	6	5
G							6	0	##
H							5	##	0

FIG. 49

FROM	TO			D	E	F	G	H
	A	B	C					
A	0	##	##					
B	##	0	##					
C	##	##	0					
D				0	##			
E				##	0	##		
F					##	0	6	5
G						6	0	##
H						5	##	0

FIG. 50

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FIG. 51

FROM	TO			D	E	F	G	H
	A	B	C					
A	0	##	##					
B	##	0	##					
C	##	##	0					
D				0	##			
E				##	0	##		
F					##	0	6	5
G						6	0	##
H						5	##	0

FIG. 52

FROM	TO			D	E	E'	F	G	H
	A	B	C						
A	0	##	##						
B	##	0	##						
C	##	##	0						
D				0	##				
E				##	0				
E'						0	##		
F						##	0	6	5
G							6	0	##
H							5	##	0

FROM	TO					
	PCI	BLOCK 2	BLOCK 1	MEMORY	BLOCK 3	PIO
PCI	0	4,100	6,100	200	0	0
BLOCK 2	10,000	0	8,000	2,000	100	100
BLOCK 1	100	10,000	0	10,000	100	100
MEMORY	100	6,000	6,000	0	100	100
BLOCK 3	200	100	200	100	0	100
PIO	0	0	0	0	0	0

FIG. 53

FROM	TO					
	PCI	BLOCK 2	BLOCK 1	MEMORY	BLOCK 3	PIO
PCI	0	4,100	6,100	200	0	0
BLOCK 2	10,000	0	8,000	2,000	100	100
BLOCK 1	100	10,000	0	10,000	100	100
MEMORY	100	6,000	6,000	0	100	100
BLOCK 3	200	100	200	100	0	100
PIO	0	0	0	0	0	0

FIG. 54

09312059-013209

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

FROM	TO	
	BUS 1	BUS 2
BUS 1	62,600	600
BUS 2	600	100

FIG. 55

FROM	TO					
	BLOCK 1	BLOCK 2	BLOCK 3	MEMORY	PCI	PIO
BLOCK 1	n/a	31	988	31	91	988
BLOCK 2	31	n/a	997	281	81	988
BLOCK 3	976	997	n/a	488	476	988
MEMORY	31	38	488	n/a	94	988
PCI	81	81	n/a	49	n/a	n/a
PIO	n/a	n/a	n/a	n/a	n/a	n/a

FIG. 56

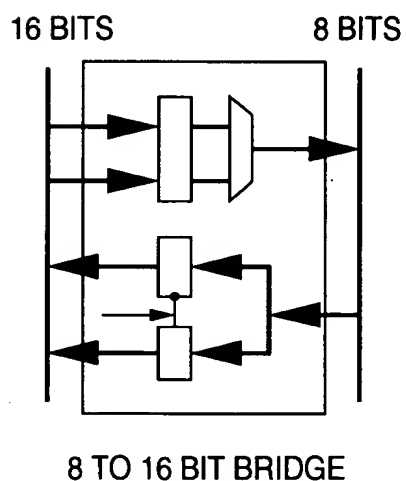


FIG. 57

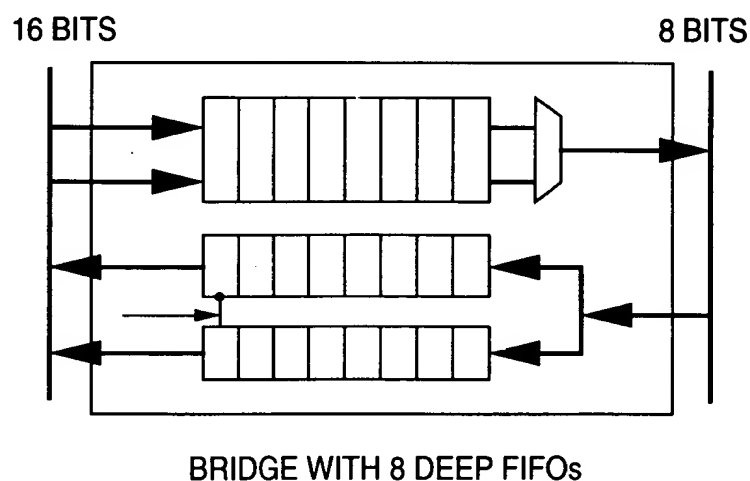


FIG. 58

09812058, 012200

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

# BUS TYPE

- SERIAL, ASYNCHRONOUS, CLOCK-REGENERATED BUS
- MULTIPLE-LINE ASYNCHRONOUS CLOCK-REGENERATED BUS
- MULTIPLE-LINE SYNCHRONOUS BUS WITH COMBINED DATA AND ADDRESS LINES
- SYNCHRONOUS BUS WITH SEPARATE DATA AND ADDRESS LINES
- BIDIRECTIONAL BUS WITH SINGLE-LEVEL PIPELINED DATA AND ADDRESS LINES
- MULTIPLE-LEVEL PIPELINED BUS WITH SOPHISTICATED ARBITRATION
- CROSSBAR SWITCH
- POINT-TO-POINT UNIDIRECTIONAL WIRE

# UTILIZATION LATENCY

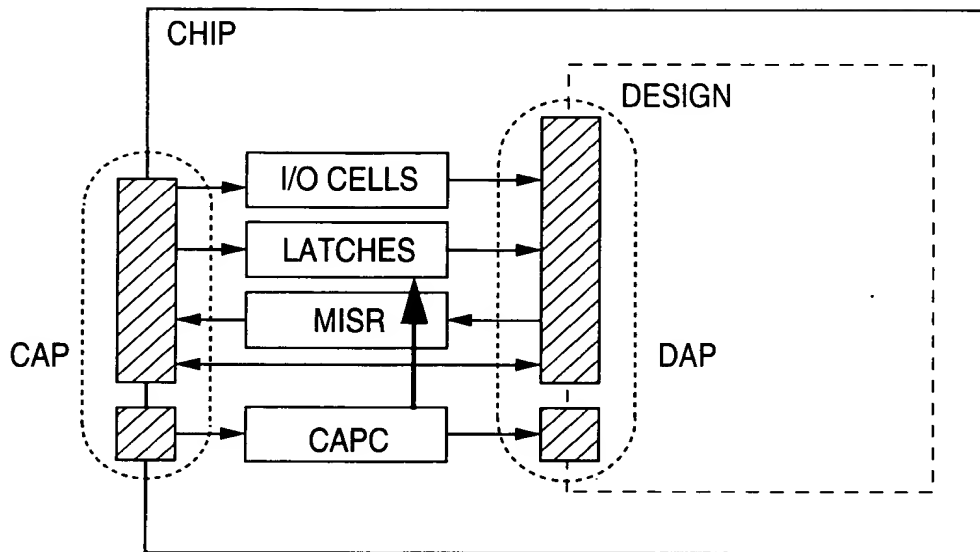
MIN	MAX	DATA	TRANSFER
5%	25%	50	200
5%	25%	20	100
10%	25%	5	25
25%	50%	2.5	10
25%	75%	2	5
50%	75%	1.5	2.5
75%	100%	1	2
100%	100%	0.5	1

**FIG. 59**

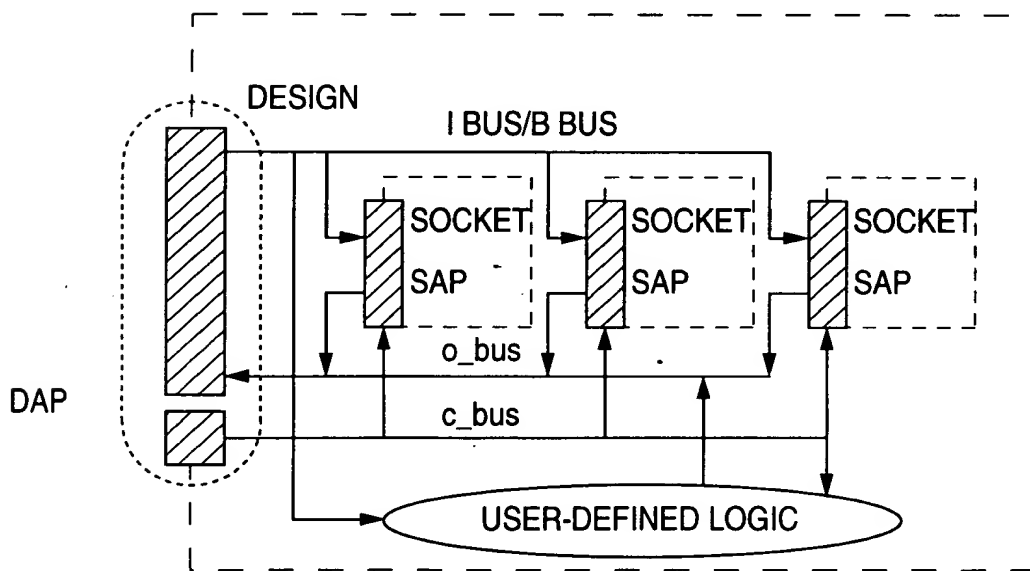
PARAMETER	NORMAL MODE	TEST MODE	ISOLATION MODE	BOUNDARY MODE
TEST MODEL	BSR MODE=0	BSR MODE=1	BSR MODE=1	BSR MODE=1
TEST CONTROLLER DESIGN	JTAG ir = bypass	JTAG ir=vc_test	JTAG ir=vc_isol	JTAG ir=udl_test
TEST ISOLATION	N/A	OUTPUT ISOLATION	INPUT ISOLATION	INPUT ISOLATION
TEST VALIDATION	FUNCTIONAL TESTBENCH	VC TEST VECTORS	INPUT ISOLATION	UPDATE BYPASS

**FIG. 60**

09812058-013202



**FIG. 61**

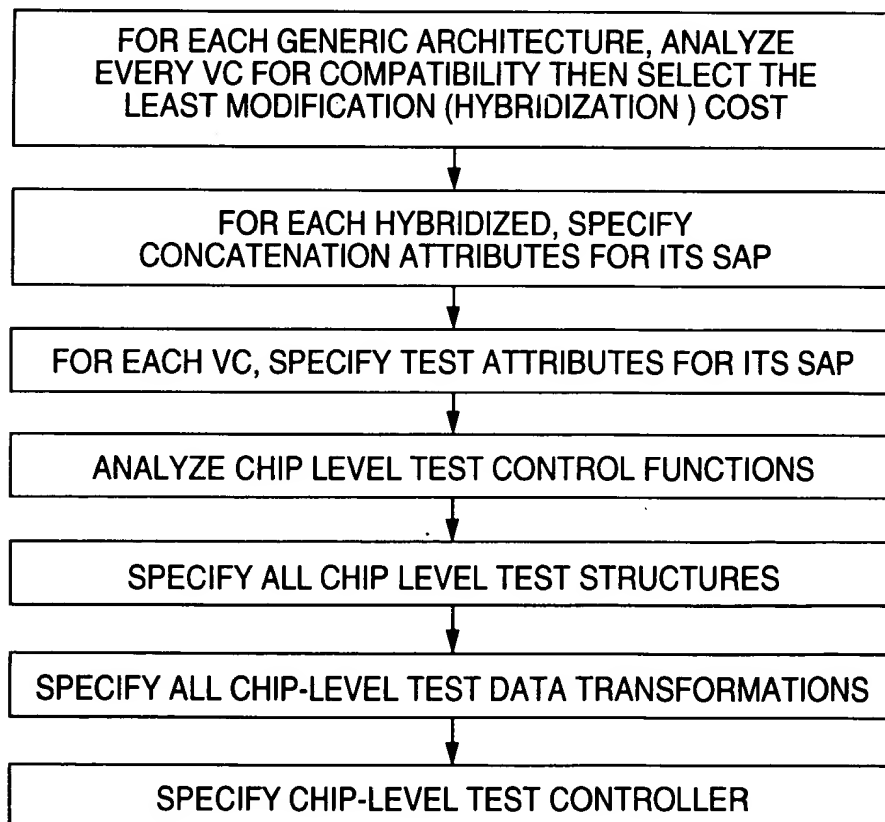


**FIG. 62**

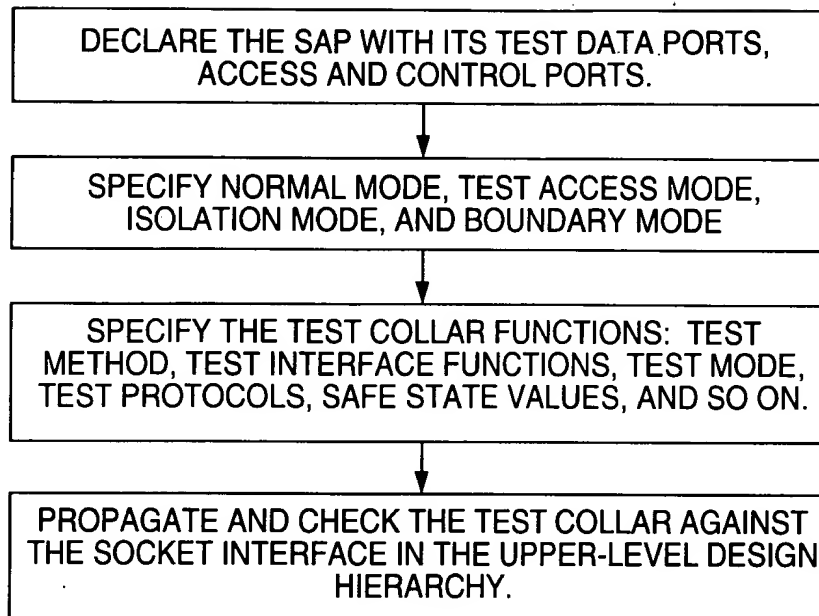
09812056 012202

GENERIC ARCHITECTURE	TARGETED BLOCKS	TEST INTERFACE	TEST METHOD
TEST BUS	LEGACY BLOCKS, NON-SCAN BLOCKS	DIRECT ACCESS FROM CHIP I/O	FUNCTIONAL VECTORS
BSR	SCAN-BASED BLOCKS	MULTIPLE SCAN + BSR CHAINS	CONCATENATED SCAN VECTORS
BIST	REGULAR BLOCKS SUCH AS RAM AND FIFO	BIST CONTROLLER	BUILT-IN ALGORITHMIC TEST PATTERNS
	BUILT-IN LOGIC BIST SUCH AS FULL SCAN	BIST CONTROLLER FOR PRPG/MISR	BUILT-IN RANDOM TEST PATTERNS
TAP	BUILT-IN DEBUG AND DIAGNOSTIC BLOCKS	TAP (TDI, TRST, TMS, TCK, TDO)	JTAG PROTOCOLS

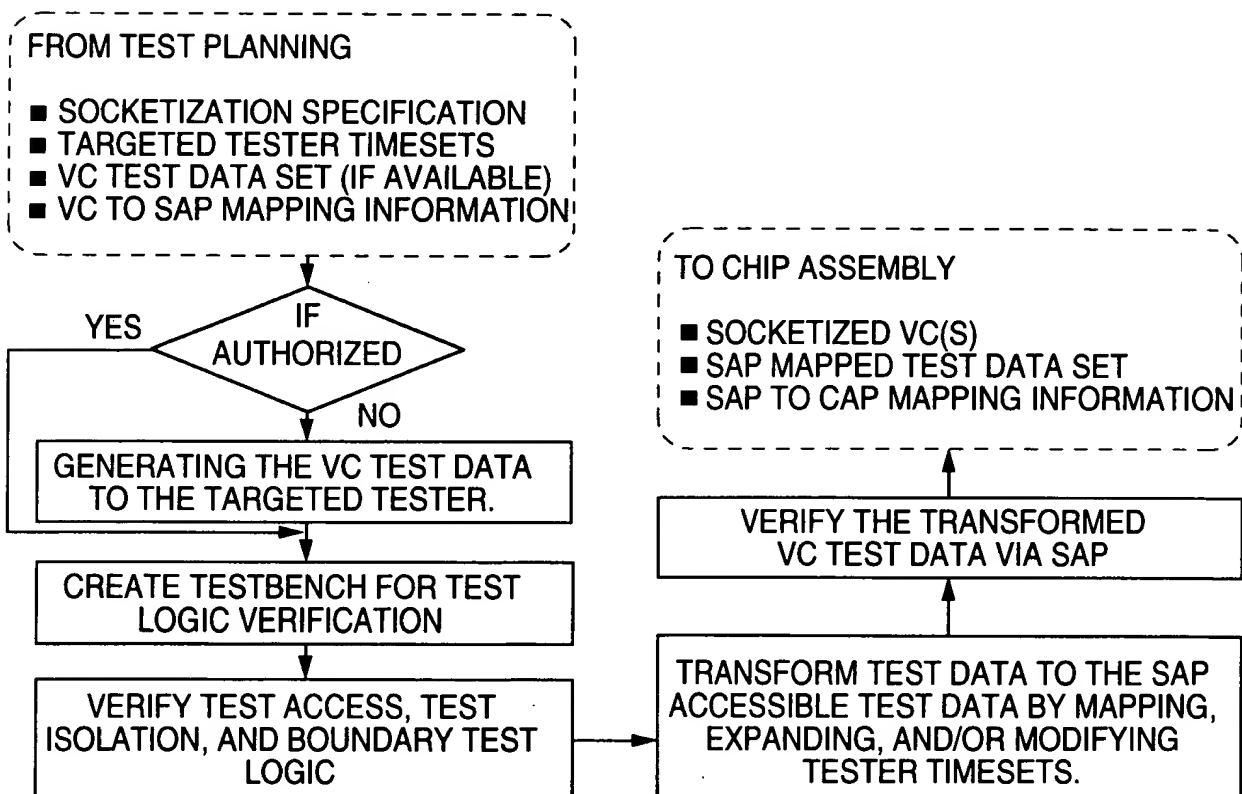
**FIG. 63**



**FIG. 64**



**FIG. 65**



**FIG. 68**

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

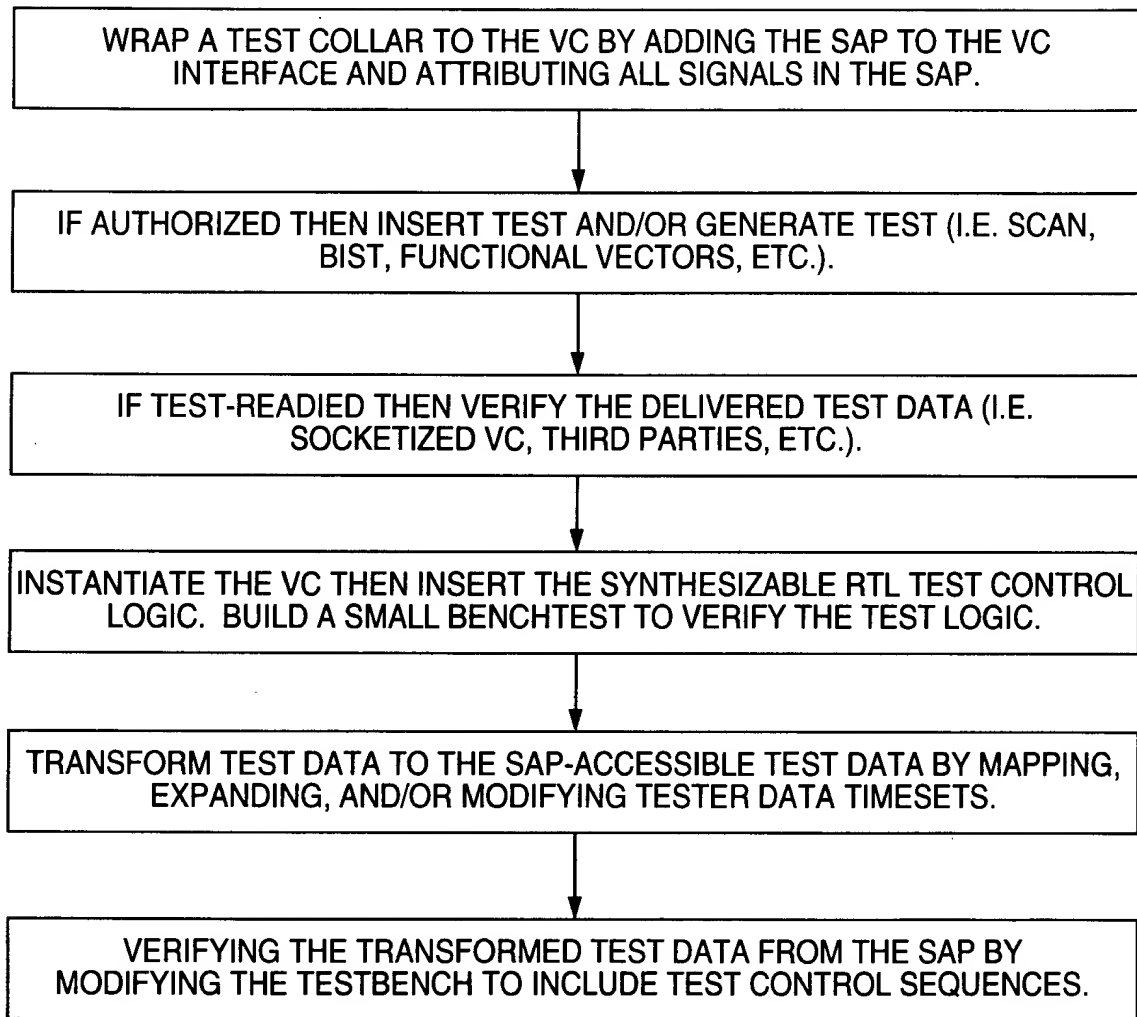


FIG. 66

00012066 012200



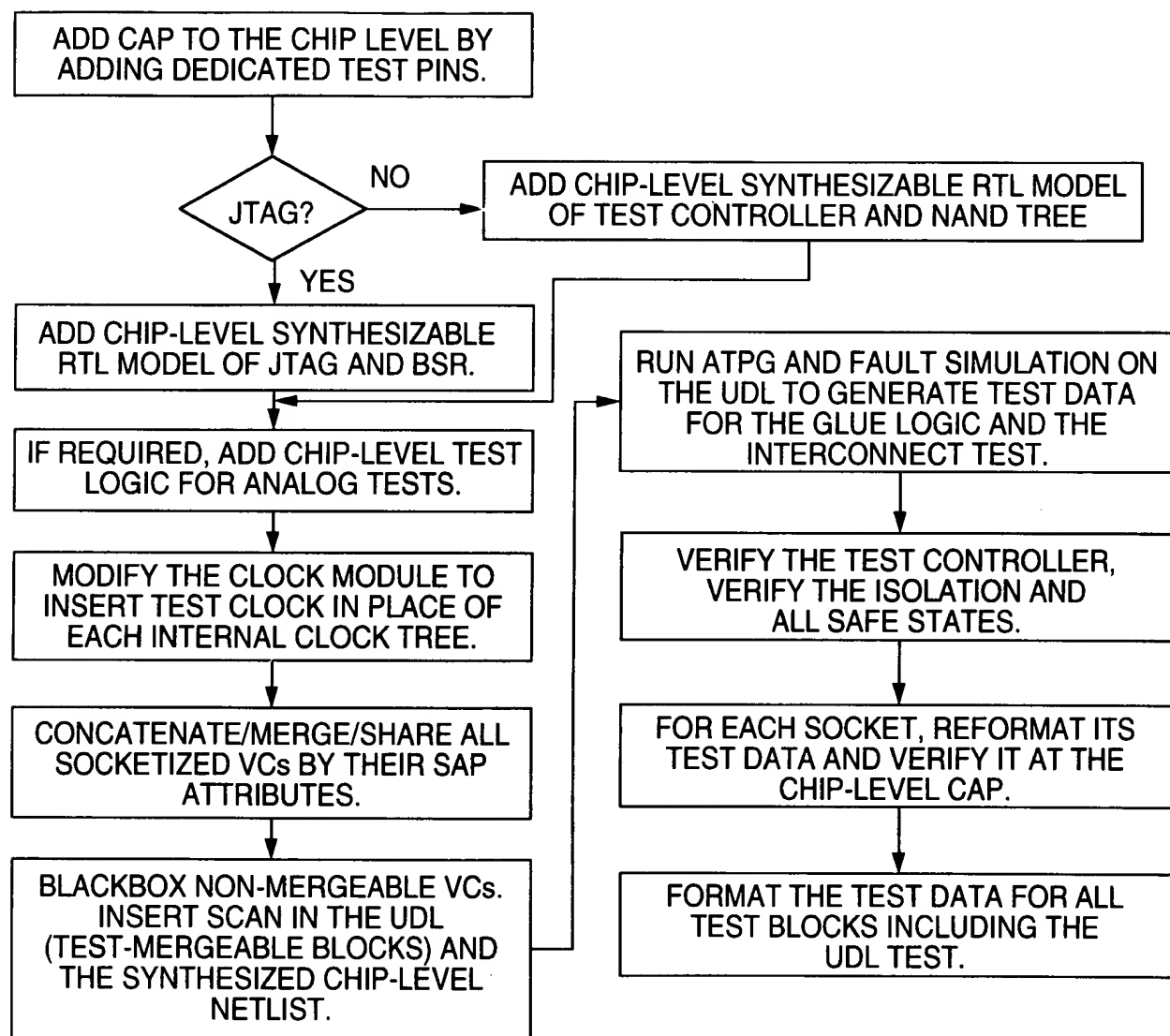
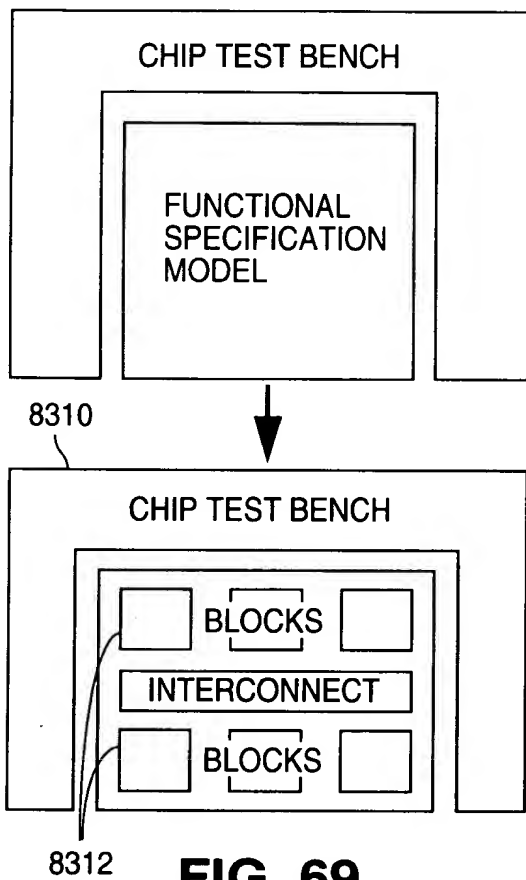
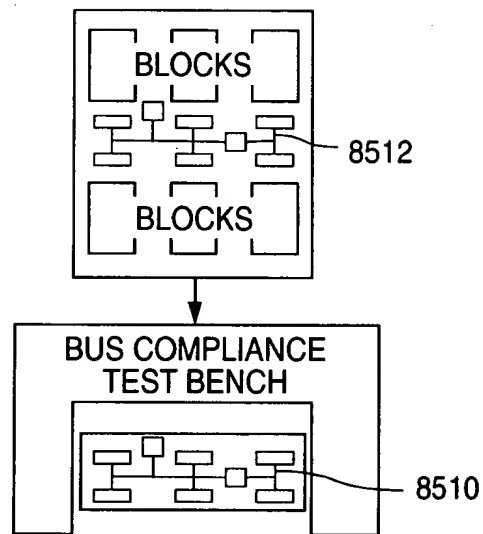


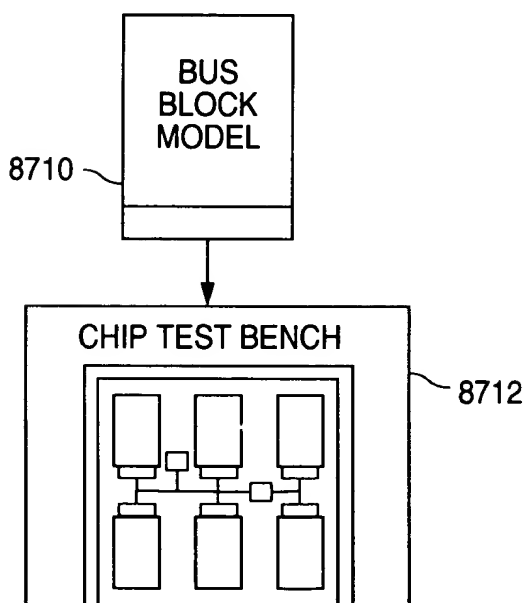
FIG. 67



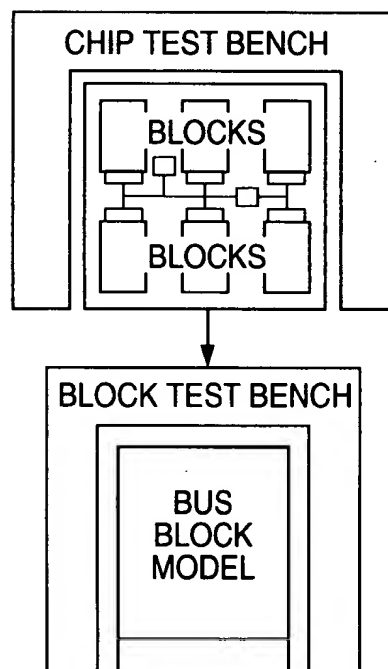
**FIG. 69**



**FIG. 70**



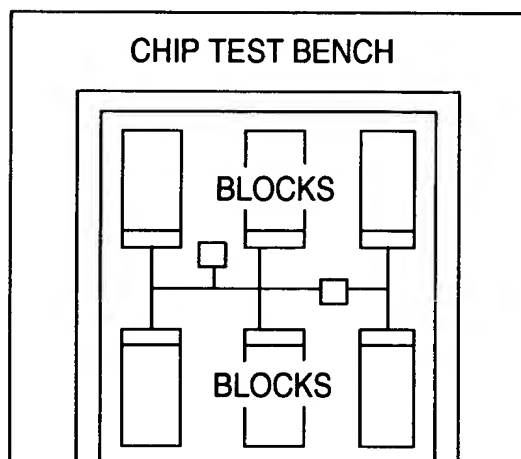
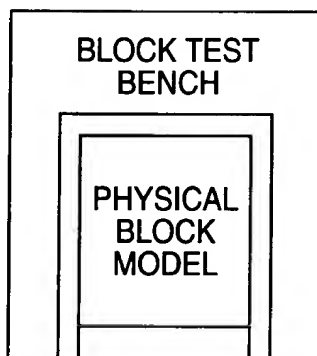
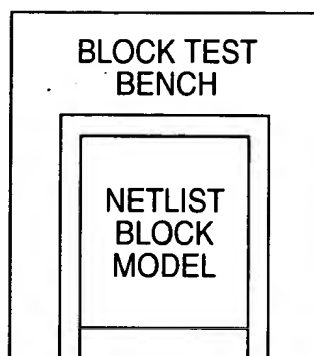
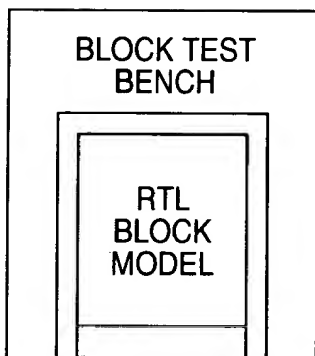
**FIG. 71**



**FIG. 72**

09812066 012200

APPROVED	O.G. FIG:	
BY	CLASS	SUBCLASS
DRAFTSMAN		



**FIG. 73**

00010000-012200

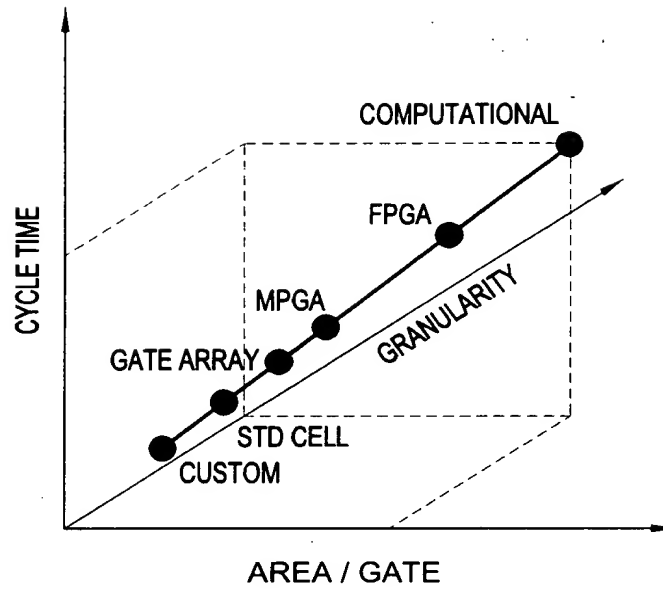


FIG. 74

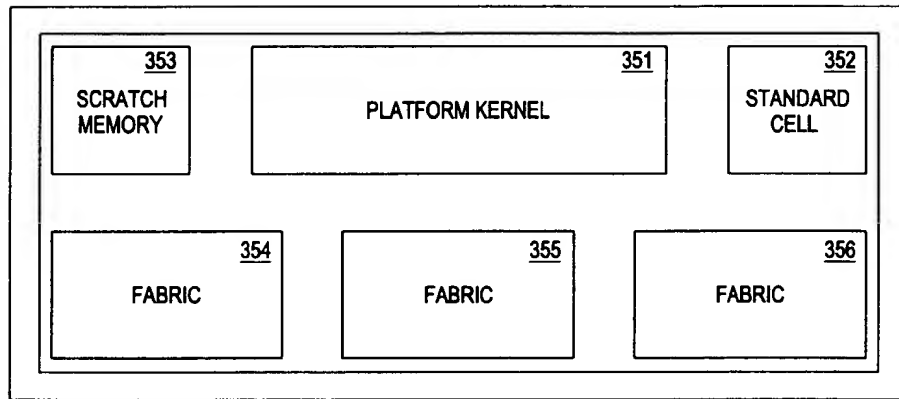


FIG. 75

350

2025-01-20 09:01:00

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

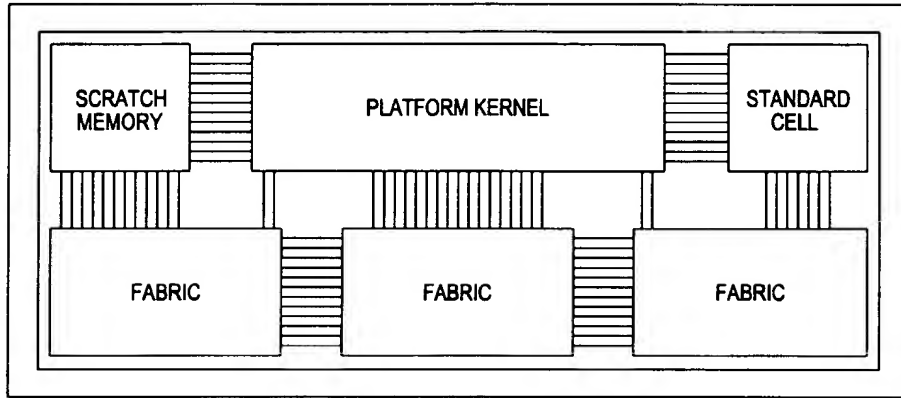


FIG. 76

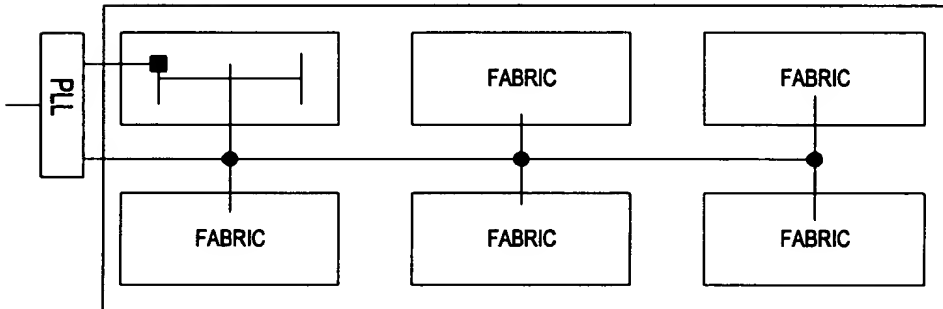
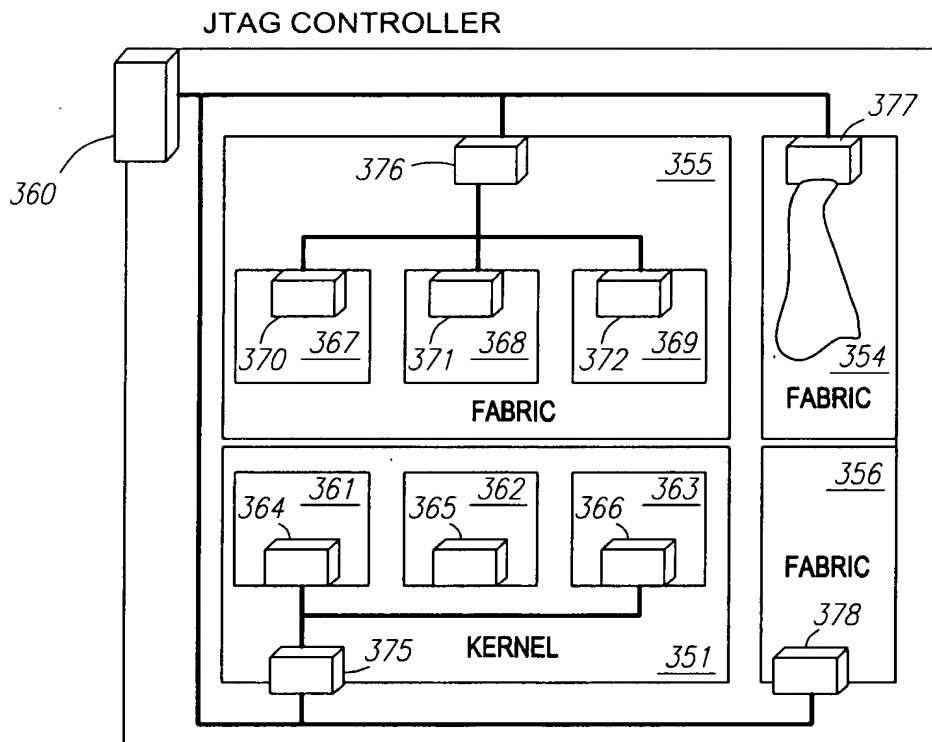


FIG. 77

00012058 "012202



*FIG. 78*

09812058-042203

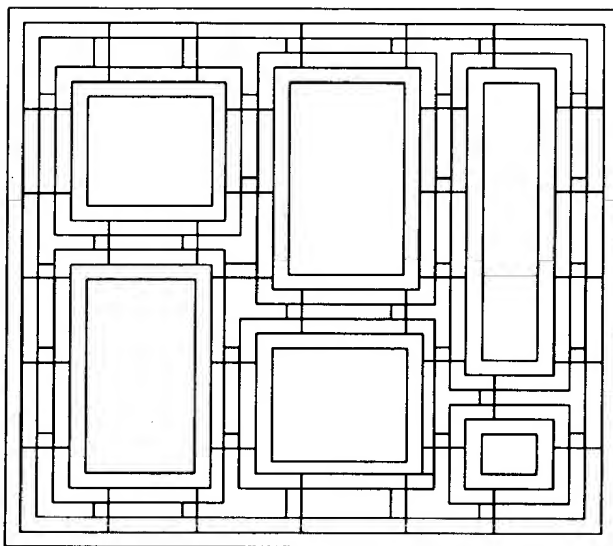


FIG. 79

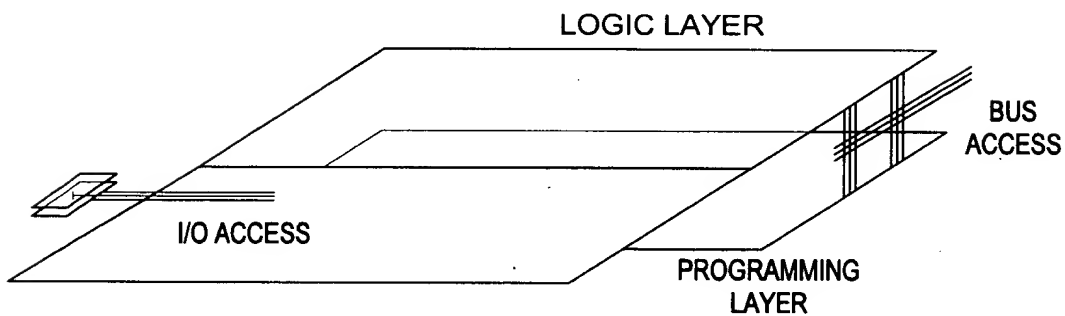


FIG. 80

09343966 012909

- EXAMPLE PLATFORM:
- 32 BIT PROCESSOR
  - A/D & D/A
  - 32/64 BIT BUS
  - USB & MEM CTRLR
  - KERNEL MODEL
  - MPGA:
  - USER CUSTOMIZED
  - SOFTWARE
  - MPGA HARDWARE

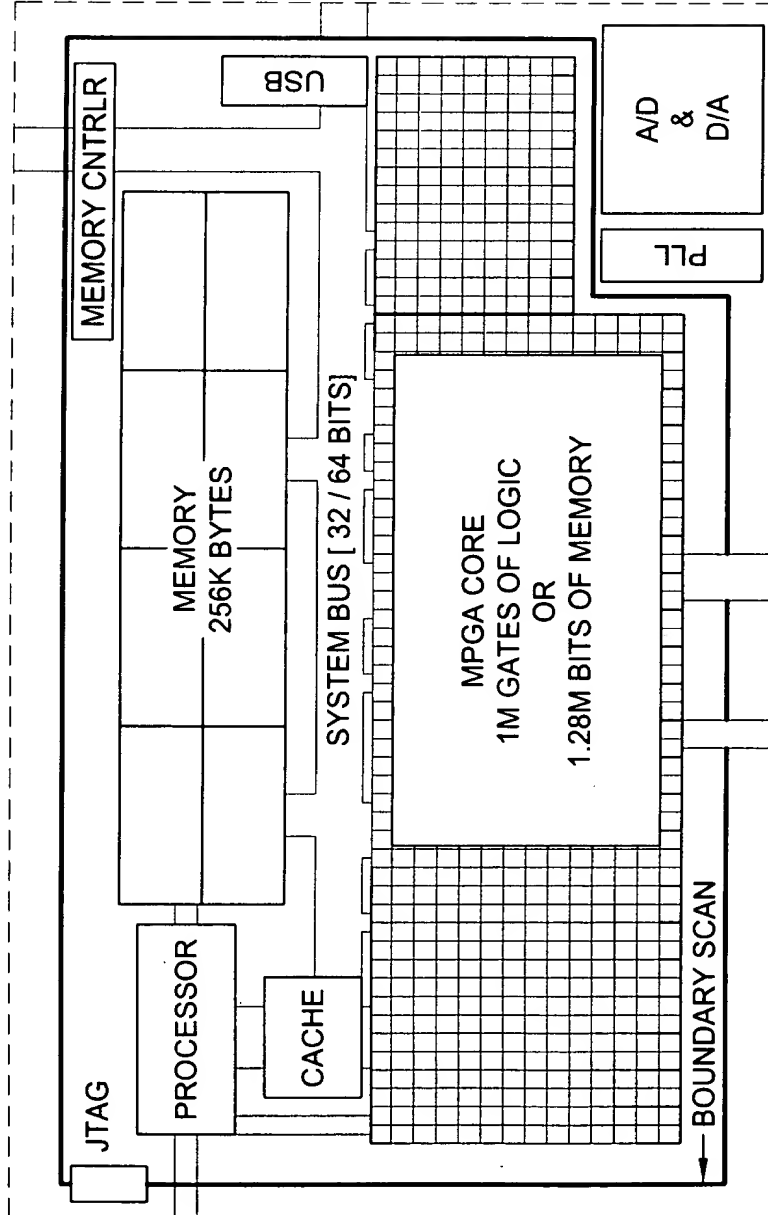


FIG. 81



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

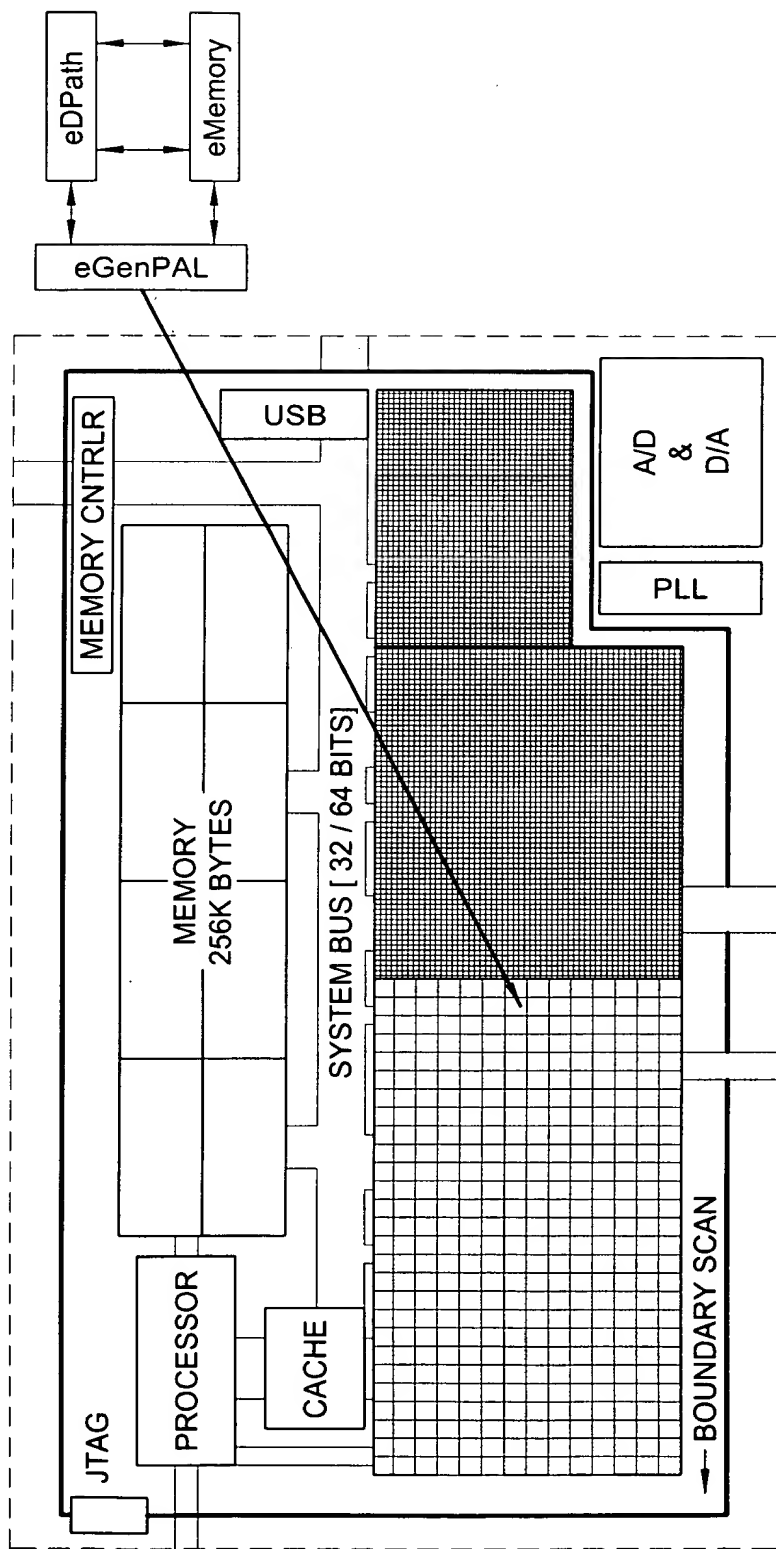


FIG. 82

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

ATTRIBUTE >	NRE	FLEXIBILITY	SIZE	POWER	PERFORMANCE	UNIT COST
FABRIC V						
CUSTOM	HIGH	LOWEST	SMALLEST	LOWEST	HIGHEST	LOWEST
STD. CELL	HIGH	LOW	SMALL	LOW	HIGH	LOW
MPGA	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM	MEDIUM
FPGA	LOW	HIGH	LARGE	HIGH	LOW	HIGH
COMPUTATIONAL	LOW	HIGHEST	LARGEST	HIGHEST	LOWEST	HIGHEST

FIG. 83

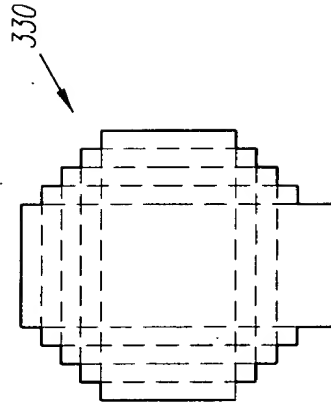


FIG. 84

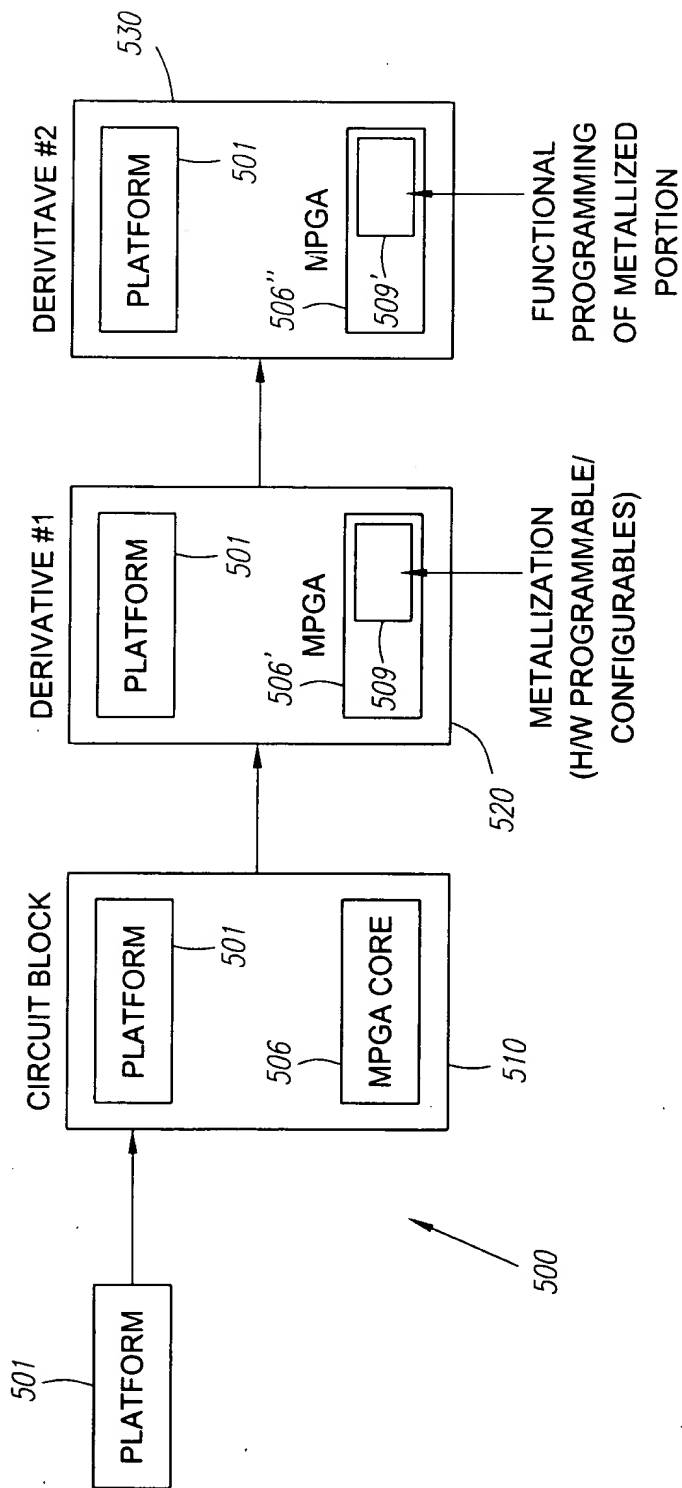
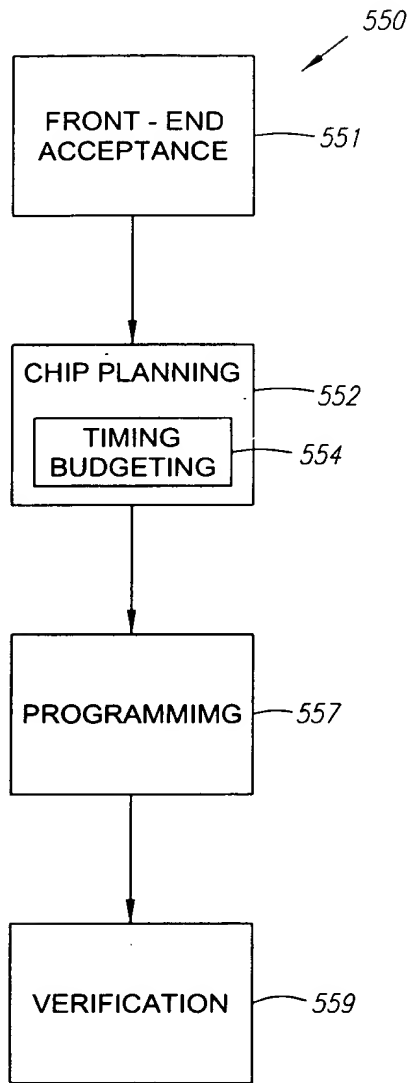
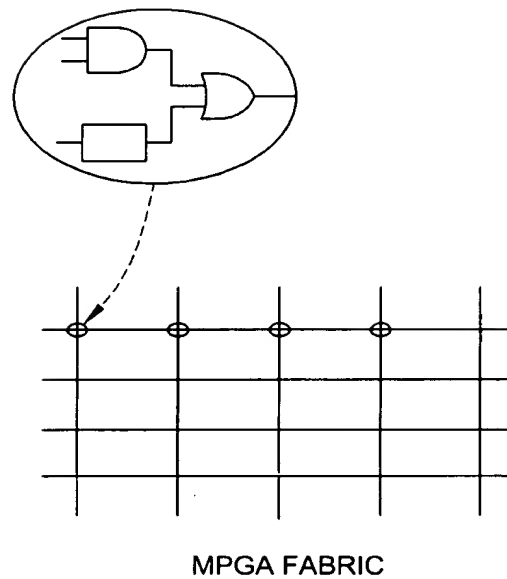


FIG. 85



DERIVATIVE DESIGN  
PROCESS FLOW

**FIG. 86**



**FIG. 87**